

Thomas F. Wenisch

Curriculum Vitae – Jun. 2009

Research Interests

High-performance computer architecture, data center architecture, multiprocessor and multicore systems, multicore programmability, performance evaluation methodology

Education

PhD in Electrical and Computer Engineering, Dec. 2007

Carnegie Mellon University, Pittsburgh, PA

- Dissertation title: Temporal Memory Streaming

MS in Electrical and Computer Engineering, May 2003

Carnegie Mellon University, Pittsburgh, PA

Bachelor of Science in Computer Engineering, Dec. 2000

Bachelor of Arts in German, Dec. 2000

University of Rhode Island, Kingston, RI

- Studied abroad at the Technische Universitaet Braunschweig, Germany in the Fall of 1999.

Honors and Awards

National Science Foundation CAREER Award, 2009-2013.

- Proposal Title: Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture.

Lamme/Westinghouse Graduate Fellowship (1 yr. full Ph.D. tuition/stipend), 2004.

Intel Ph.D. Research Fellowship (1 yr. full Ph.D. tuition/stipend), 2003.

Honorable Mention, National Science Foundation Graduate Research Fellowship, 2002.

Laboratory for Computer Systems Fellowship, Carnegie Mellon University (1 yr. full Ph.D. tuition/stipend), 2001.

President's Award in Computer Engineering, University of Rhode Island, 2000.

Centennial Scholarship, University of Rhode Island, 1996-2000.

Refereed Conference Papers

C. Blundell, M. M. K. Martin, T. F. Wenisch. "InvisiFence: Performance-Transparent Memory Ordering in Conventional Multiprocessors." *Proc., of the 36th International Symposium on Computer Architecture (ISCA)*, Jun. 2009.

K. Lim, J. Chang, T. Mudge, P. Ranganathan, S. K. Reinhardt, T. F. Wenisch. "Disaggregated Memory for Expansion and Sharing in Blade Servers." *Proc., of the 36th International Symposium on Computer Architecture (ISCA)*, Jun. 2009.

S. Somogyi, T. F. Wenisch, A. Ailamaki, and B. Falsafi. "Spatio-Temporal Memory Streaming." *Proc., of the 36th International Symposium on Computer Architecture (ISCA)*, Jun. 2009.

D. Meisner, B. T. Gold, and T. F. Wenisch. "PowerNap: Eliminating Server Idle Power." To Appear in *Proc. of the 14th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Mar. 2009.

T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi and A. Moshovos. "Practical Off-chip Meta-data for Temporal Memory Streaming." To Appear in *Proc. of the 15th International Symposium on High-Performance Computer Architecture (HPCA)*, Feb. 2009.

M. Ferdman, T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Temporal Instruction Fetch Streaming." *Proc. of the 41st Annual International Symposium on Microarchitecture (MICRO)*, Dec. 2008.

- T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi and A. Moshovos. "Temporal Streams in Commercial Server Applications." *Proc. of the IEEE International Symposium on Workload Characterization (IISWC)*, 2008.
- T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Mechanisms for Store-wait-free Multiprocessors." *Proc. of the 34th International Symposium on Computer Architecture (ISCA)*, Jun. 2007.
- S. Somogyi, T. F. Wenisch, A. Ailamaki, B. Falsafi and A. Moshovos. "Spatial Memory Streaming." *Proc., of the 33rd International Symposium on Computer Architecture (ISCA)*, Jun. 2006.
- T. F. Wenisch, R. E. Wunderlich, B. Falsafi and J. C. Hoe. "Simulation Sampling with Live-Points." *Proceedings of the International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Mar. 2006.
- T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki, and B. Falsafi. "Store-Ordered Streaming of Shared Memory." *Proc. of the 14th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, Sep. 2005.
- T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, A. Ailamaki, and B. Falsafi. "Temporal Streaming of Shared Memory." *Proc. of the 32nd International Symposium on Computer Architecture (ISCA)*, Jun. 2005.
- T. F. Wenisch, R. E. Wunderlich, B. Falsafi, and J. C. Hoe. "TurboSMARTS: Accurate Microarchitecture Simulation Sampling in Minutes." (Short paper) *Proc. of the International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS)*, Jun. 2005.
- R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "SMARTS: Accelerating Microarchitecture Simulation via Rigorous Statistical Sampling." *Proc. of the 30th International Symposium on Computer Architecture (ISCA)*, Jun. 2003.
- T. F. Wenisch, P. F. Swaszek and A. K. Uht. "Combined Error Correcting and Compressing Codes." *Proc. of the International Symposium on Information Theory (ISIT)*, Jun. 2001.

Journal Articles

- T. F. Wenisch, R. E. Wunderlich, M. Ferdman, A. Ailamaki, B. Falsafi, and J. C. Hoe. "SimFlex: Statistical Sampling of Computer System Simulation." *IEEE MICRO Special Issue on Computer Architecture Simulation and Modeling*, vol. 26, no. 4, Jul./Aug. 2006.
- R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "Statistical Sampling of Microarchitecture Simulation." *ACM Transactions on Modeling of Computer Systems (TOMACS)*, vol. 16, no. 3, Jul. 2006.
- N. Hardavellas, S. Somogyi, T. F. Wenisch, R. E. Wunderlich, S. Chen, J. Kim, B. Falsafi, J. C. Hoe, A. Nowatzyk. "SimFlex: A Fast, Accurate, Flexible Full-System Simulation Framework for Performance Evaluation of Server Architecture." *ACM SIGMETRICS Performance Evaluation Review (PER)*, Vol. 31, No. 4, Mar. 2004.
- A. K. Uht, D. Morano, A. Khalafi, M. de Alba, T. F. Wenisch, M. Ashouei and D. Kaeli. "Levo: IPC in the 10's via Resource Flow Computing." *IEEE Technical Committee on Computer Architecture Newsletter*, Special Issue: Oct. 2001.

Workshop Papers

- S. Pelley, D. Meisner, T. F. Wenisch, and J. VanGilder. "Understanding and Abstracting Total Data Center Power." *Proc. of the Workshop on Energy Efficient Design (WEED)*, Jun. 2009.
- T. F. Wenisch, R. E. Wunderlich, B. Falsafi, and J. C. Hoe. "Statistical Sampling of Microarchitecture Simulation." *Proc. of the 2006 Workshop on the NSF Next Generation Software Program (NGS)*, Apr. 2006.
- S. Somogyi, T. F. Wenisch, N. Hardavellas, J. Kim, A. Ailamaki, and B. Falsafi. "Memory Coherence Activity Prediction in Commercial Workloads." *Proc. of the 3rd Workshop on Memory Performance Issues (WMPI)*, Jun. 2004.
- R. E. Wunderlich, T. F. Wenisch, B. Falsafi, and J. C. Hoe. "An Evaluation of Stratified Sampling of Microarchitecture Simulations." *Proc. of the 3rd Workshop on Duplicating, Debunking, and Deconstructing (WDDD)*, Jun. 2004.

Technical Reports

- T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. C. Hoe, "TurboSmarts: Accurate Microarchitecture Simulation Sampling in Minutes," Technical Report 2004-3, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Nov. 2004.
- T. F. Wenisch, S. Somogyi, N. Hardavellas, J. Kim, C. Gniady, A. Ailamaki, and B. Falsafi. "SORDS: Just-In-Time Streaming of Temporally-Correlated Shared Data," Technical Report 2004-2, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Nov. 2004.
- T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. C. Hoe, "Applying SMARTS to SPEC CPU2000," Technical Report 2003-1, Computer Architecture Laboratory at Carnegie Mellon University (CALCM), Jun. 2003.

Patents

- D. Meisner, T. F. Wenisch. "Computer Energy Conservation with a Scalable PSU Configuration". US Patent Pend., Filed 12/16/2008.
- T. F. Wenisch, S. R. Berard, D. J. Smith. "Computer Network Security System". US Patent No. 7,100,054. Issued 8/29/2006.
- T. F. Wenisch. "Software-based Watchdog Method and Apparatus." US Patent No. 7,162,714. Issued 1/9/2007.
- C. Kuiawa, D. Cardimino, T. Giaquinto, T. F. Wenisch. "Uninterruptible Power Supply Management Network System". US Patent Pend., Appl. No. 20030033548. Filed 8/9/2001.

Presentations

- "Thinking Outside the Box." International Symposium on Low Power Electronic Design (ISLPED) (Invited Plenary Talk), Aug. 2009.
- "Making Enterprise Computing Green." Yahoo! HKN Seminar Series, Mar. 2009.
- "Making Enterprise Computing Green." Merit Member Conference, Jun. 2009.
- "Making Enterprise Computing Green." Tutorial at the International Conference on High-Performance Computing (HiPC), Dec. 2008.
- "Improving Memory System Performance and Eliminating Idle-power Waste in Commercial Servers." Intel Research Bangalore, Dec. 2008.
- "Hiding Memory Latency in Commercial Server Application." Indian Institute of Science, Dec. 2008.
- "Mechanisms for Store-Wait-Free Multiprocessors." ARM, Nov. 2008.
- "Making Enterprise Computing Green: Energy-efficiency Challenges in Enterprise Data Centers." Carnegie Mellon University, Oct. 2008.
- "Hiding Memory Latency in Commercial Server Application." IBM TJ Watson, Jul. 2008.
- "Mechanisms for Store-Wait-Free Multiprocessors." 34th International Symposium on Computer Architecture (ISCA), Jun. 2007.
- "Temporal Memory Streaming." University of Toronto, University of Michigan, MIT, Columbia University, UT-Austin, Microsoft Research-Silicon Valley, Microsoft Research-Redmond, HP Labs in Feb.-Apr. 2007.
- "Improving the Simulation and Programmability of Future Multiprocessor Systems." Brown University, Jan 2007.
- "SimFlex: Simulation Sampling Theory and Practice." University of Pittsburgh, Feb. 2006.
- "Store-Ordered Streaming of Shared Memory." 14th International Conference on Parallel Architectures and Compilation Techniques (PACT), Sep. 2005.
- "Temporal Streaming of Shared Memory." 32nd International Symposium on Computer Architecture (ISCA), Jun. 2005.
- "TurboSMARTS: Accelerating Microarchitecture Simulation Sampling in Minutes." Princeton, Sep. 2004.
- "Breaking the Memory Wall." Intel, Santa Clara, CA, Oct. 2003.
- "SMARTS: Accelerating Microarchitecture Simulation via Rigorous Statistical Sampling." 30th International Symposium on Computer Architecture (ISCA), Jun. 2003.
- "Combined Error Correcting and Compressing Codes" International Symposium on Information Theory (ISIT), Jun. 2001.

Press Coverage	<p>“PowerNap plan could save 75 percent of data center energy.” University of Michigan News Service, 3/5/09</p> <p>“‘Napping’ data centers could cut energy use by 75 percent.” ZDNet Asia, 3/6/09.</p> <p>“Optimizing The Sleep Cycle.” Processor.com, 6/5/09.</p> <p>“Merit Member Conference Covers Cool Learning Technology.” WWJ Radio, 6/11/09.</p>															
Grants and Awards	<p>CAREER: Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture (NSF; CCF-0845157; T. Wenisch–PI; \$400,000; 2009-2013)</p> <p>Programming Interfaces and Hardware Designs for a Polymorphic Multicore Cache Architecture (Intel; \$80,000; 2009-2010)</p> <p>CSR-DMSS,SM: Beyond Solid State Disks: Using FLASH to save energy in Enterprise Systems (NSF; CSR-0834403; T. Wenisch–PI, T. Mudge–Co-PI; \$280,000; 2008-2011)</p> <p>CPA-CSA: Virtualization Mechanisms for Zero-Idle-Power and Thermally-Efficient Data Centers (NSF; CCF-0811320; T. Wenisch–PI; \$275,000; 2008-2011)</p> <p>Disaggregated Memory for Energy-Efficient Data Centers (HP Labs; T. Mudge–PI, T. Wenisch–Co-PI; \$145,000; 2008-2009)</p> <p>FloVent License Grant (Flomerics; \$9,600; 2008-2009)</p> <p>Equipment Donation (Intel;\$30,000; 2008)</p>															
Professional Activities	<p>Co-organizer of the Fifth Annual Workshop on Modeling, Benchmarking, and Simulation (MoBS), held in conjunction with ISCA 2009.</p> <p>Tutorial presentation: T. F. Wenisch. “Making Enterprise Computing Green”. Held in conjunction with HiPC 2008 (Bangalore, India).</p> <p>Tutorial presentation: T. F. Wenisch, R. E. Wunderlich, B. Falsafi, J. Hoe. “SimFlex: Fast, Accurate and Flexible Simulation of Computer Systems”. Held in conjunction with: 38th Annual International Symposium on Microarchitecture (MICRO), Nov. 2005 33rd International Symposium on Computer Architecture (ISCA), Jun. 2006.</p> <p>Panelist: “Cycle-Accurate Simulators: Knowing When to Say When.” held in conjunction with ISCA (2008).</p> <p>Principal developer of the Flexus full-system multiprocessor computer architecture simulation framework, publicly available at http://www.ece.cmu.edu/~simflex.</p> <p>Principal developer of the TurboSmartsim simulation sampling & checkpointing extensions to SimpleScalar, publicly available at http://www.ece.cmu.edu/~simflex.</p> <p>Finance chair for PACT (2008).</p> <p>Publications chair for MICRO (2009).</p> <p>Technical Program Committee Member for TRANSACT (2008), MOBS (2008), CMP-MSI (2008), DATE Architecture track (2008), WISH (2009), ISPASS (2009, 2010), ICS (2009), WEED (2009), PACT (2009), HotPower (2009).</p> <p>External reviewer for ACM TACO, ACM TOCS, ACM TECS, IEEE JILP, ISPASS (2004), ICS (2005), PACT (2005), ISCA (2006, 2007, 2008,2009), TRANSACT (2007), ASPLOS (2007, 2009), MICRO (2008), HPCA (2008, 2009).</p> <p>Member of the ACM and IEEE.</p>															
Employment History	<table border="0"> <tr> <td style="vertical-align: top;">9/2007</td> <td style="vertical-align: top;">University of Michigan</td> <td style="vertical-align: top;">Ann Arbor, MI</td> </tr> <tr> <td></td> <td style="vertical-align: top;">Assistant Professor, Computer Science & Engineering</td> <td></td> </tr> <tr> <td style="vertical-align: top;">9/2006</td> <td style="vertical-align: top;">AuthenTec</td> <td style="vertical-align: top;">Melbourne, FL</td> </tr> <tr> <td></td> <td style="vertical-align: top;">Security Consultant</td> <td></td> </tr> <tr> <td></td> <td colspan="2"> <ul style="list-style-type: none"> • Provided independent review of a proposed biometric authentication system architecture. </td> </tr> </table>	9/2007	University of Michigan	Ann Arbor, MI		Assistant Professor, Computer Science & Engineering		9/2006	AuthenTec	Melbourne, FL		Security Consultant			<ul style="list-style-type: none"> • Provided independent review of a proposed biometric authentication system architecture. 	
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	Assistant Professor, Computer Science & Engineering															
9/2006	AuthenTec	Melbourne, FL														
	Security Consultant															
	<ul style="list-style-type: none"> • Provided independent review of a proposed biometric authentication system architecture. 															

9/2000 – 9/2006

American Power Conversion

West Kingston, RI

Software Developer

- Developed network management software for uninterruptible power supplies.
- Designed novel security mechanisms for web-based user interfaces (US patent 7,100,054).

2/2000 – 8/2000

Siemens AG

Munich, Germany

Test Engineer (intern)

- Created test hardware and software for subscriber line modules for ISDN switching systems.
- Developed a PC expansion card and accompanying device drivers for controlling custom measurement hardware.

Teaching

EECS 598 – Enterprise Systems (Winter 2008)

EECS 470 – Computer Architecture (Fall 2007, Winter 2009)