EECS 470 Lab 4 Assignment

Note:

- The lab should be completed individually.
- The lab must be submitted by the end of Thursday office hours the following week and checked off by a GSI.

1 Introduction

You have been supplied with three, obfuscated, buggy ISR modules. These modules should implement the ISR functionality from Project 2 correctly, however they are not quite right. The supplied ISRs are using a 4-cycle version of the pipelined multiplier. The module has the regular definition:

```
module ISR(reset, value, clock, result, done);
```

2 Assignment

For this lab, you will need to write a testbench that will catch all the three buggy modules. Your testbench must use a task to check the solution of the ISR module (this is not that easy to do). See the testbenches from the previous labs if you do not remember how to write a task.

In addition to catching the bugs, you must figure out what the source of each bug is. This will require you to think critically. Since you do not have access to the source of the module, you will have to look at its outputs and try to theorize what could be causing the errors you are seeing. This is not easy, you will have to think hard about how the ISR should work and how that compares to what you are seeing.

_Hint:_ The bugs in _buggy1_ and _buggy3_ are in the ISR module. The bug in _buggy2_ is in one of the submodules.

3 Check Off

In order to get your work checked off, you will need to type up your explanation of each bug for a GSI to read. Once you have done this, please add yourself to the help queue and mark that you wish to be checked off.