QED: Quick Error Detection Tests for Effective Post-Silicon Validation

Jiong Xue
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Outline

• Background

• Proposed Solution - QED
  • EDDI-V
  • RMT-V

• Experimental Evaluation
  • Hardware experimental results
  • Simulation results

• Conclusion
Background

- Post-Silicon Validation
- Electrical Bugs
- Error Detection Latency

Core 1

A ← B + 8
Mem[C] ← A

Core 2

D ← Mem[C]
E ← Mem[D]

SEGFAULT

Inter-core store-to-load latency
Motivation

Long latencies limit the effectiveness of debug
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  • EDDI-V (Error Detection by Duplicated Instructions for Validation)
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EDDI-V

Duplicate instructions and compare the results

Original Code

QED Code

Error

Long error detection latency

Short error detection latency
EDDI-V Implementation

Reserve half of general purpose registers

Init:
A ← 5
B ← 1
C ← 3
D ← 0xf

Body:
A ← A + B
C ← D - B

Init:
A ← 5
A' ← 5

Body:
A ← A + B
C ← D - B

A' ← A' + B'
C' ← D' - B'
Check A == A'
Check C == C'

:
EDDI-V Implementation

Reserve half of memory

Init:
A ← 5
B ← 1
C ← 3
D ← 0xf

Body:
(A,B,C,D) ← MEM[0:3]
A ← A + B
C ← D - B
MEM[4:7] ← (A,B,C,D)

Init:
MEM[0:3] ← {5,1,3,0xf}
MEM[4:7] ← {5,1,3,0xf}

Body:
(A,B,C,D) ← MEM[0:3]
A ← A + B
C ← D - B
MEM[0:3] ← (A,B,C,D)
(A,B,C,D) ← MEM[4:7]
A ← A + B
C ← D - B
Check A == MEM[0]
Check C == MEM[2]
MEM[4:7] ← (A,B,C,D)

::
EDDI-V Advantages

• Inst_min vs Inst_max
  • Minimum and maximum of original instructions inserted before QED code

• Bounded error detection latency

• Tradeoff between latency and intrusiveness
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RMT-V

Duplicate the original thread

Main thread

Init:
A \leftarrow 0
B \leftarrow 0
C \leftarrow 0
D \leftarrow 0

Body:
J \leftarrow A + B
K \leftarrow C - D
STORE J
ENQUEUE J
ENQUEUE K

Check thread

Init:
A \leftarrow 0
B \leftarrow 0
C \leftarrow 0
D \leftarrow 0

Body:
J' \leftarrow A' + B'
K' \leftarrow C' - D'
STORE J'
DEQUEUE J
DEQUEUE K
CHECK J == J'
CHECK K == K'

FIFO
RMT-V Implementations

- Software RMT-V (S-RMT-V)
  - Lock-free queues implemented in software
  - Three instructions per enqueue operation
- S-RMT-V with Hardware Queues (S-RMT-V-HQ)
RMT-V Implementations

- Hardware RMT-V (H-RMT-V)
  - Monitor automatically enqueues the results
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Hardware Experiments

• Quad-core Intel Core i7 Processor Platform
• Voltage and frequency can be changed
• Temperature remains constant
Error Detection Latency Results

- Error detection latencies ↓ by six orders of magnitude
- Masked errors can be detected
### Electrical Bug Coverage Analysis

<table>
<thead>
<tr>
<th>Voltage (1.0125V - 1.1500V)</th>
<th>Frequency (3.2GHz - 3.7GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>QED</td>
<td>Did not boot</td>
</tr>
<tr>
<td>1.0 1.0 0.1</td>
<td>Error detected</td>
</tr>
<tr>
<td>1.0 0.3</td>
<td>Error detected by QED, pass for Non QED</td>
</tr>
<tr>
<td>Non QED</td>
<td>Pass</td>
</tr>
<tr>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>1.0 0.7 0.2</td>
<td></td>
</tr>
<tr>
<td>0.6 0.3</td>
<td></td>
</tr>
</tbody>
</table>

- QED can improve coverage
- Coarse-grained assertions may not be sufficient to reduce error detection latencies
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Simulation Experiments

• 4-core 4-way out-of-order MIPS processor

• Goal:
  • Estimate error detection latency
  • Characterize error detection latency for H-RMT-V
Simulation Results

• Latencies are within 1k cycles
• Simulation results are consistent with hardware experimental results
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Conclusion

- Improve error detection latencies by six orders of magnitude
- Improve the coverage of post-silicon validation tests
Questions?
Debate

• Since QED detects only electrical bugs, is it good to combine QED with ISA diversity method?

• Which approach is better, EDDI-V or RMT-V?
Thank you!
Backup
Error Detection Latency Measure

\[ t = t_0 \]

- Error manifested
- Error Detected
Error Detection Latency Measure

t = t_0
t = t_0 + \Delta

Error manifested

Error Detected
Error Detection Latency Measure

- $t = t_0$
- $t = t_0 + \Delta$
- $t = t_0 + 2\Delta$
- Error manifested
- Error Detected
Error Detection Latency Measure

\[ t = t_0 \]
\[ t = t_0 + \Delta \]
\[ t = t_0 + 2\Delta \]
\[ t = t_0 + 3\Delta \]

No error detected
Error Detection Latency Measure

Injection-to-detect latency

$t = t_0$
$t = t_0 + \Delta$
$t = t_0 + 2\Delta$
Error manifested
Error Detected