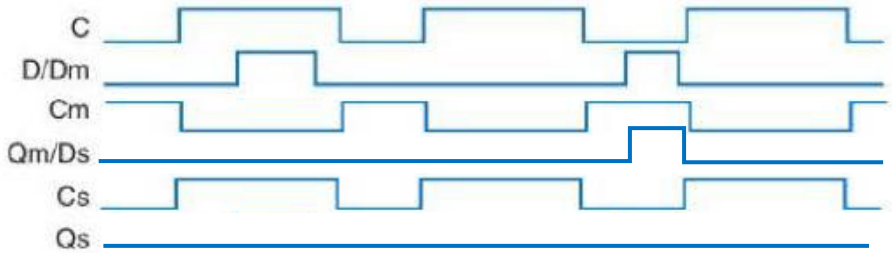
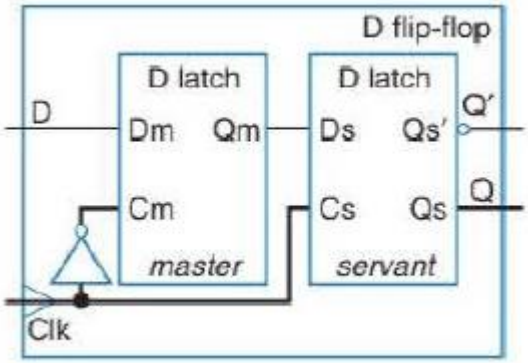
1)

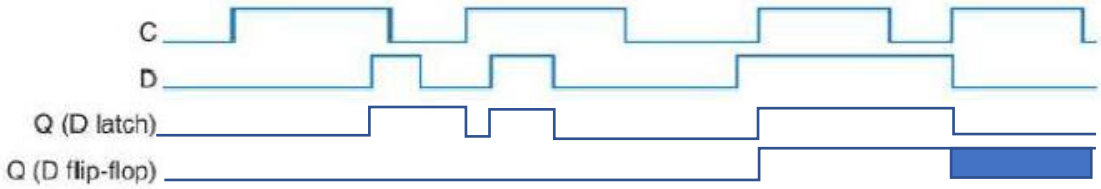
3.13 Trace the behavior of an edge-triggered D flip-flop using the master-servant design (see Figure 3.25) for the input pattern in Figure 3.100. Assume each internal latch initially stores a 0. Complete the timing diagram, assuming logic gates have a tiny but nonzero delay.





2)

3.15 Compare the behavior of D latch and D flip-flop devices by completing the timing diagram in Figure 3.102. Assume each device initially stores a 0. Provide a brief explanation of the behavior of each device.



3)

s_1	s_0	a	b	s_1'	s_0'
0	0	1	X	0	0
0	0	0	1	0	1
0	0	0	0	1	0
0	1	1	X	1	0
0	1	0	X	0	1
1	0	X	1	1	1
1	0	X	0	1	0
1	1	X	X	0	0

$$s_1' = s_1 s_0' + s_1' s_0 a + a' b' s_1' s_0'$$

$$s_0' = s_1' s_0' a' b + s_1' s_0 a' + s_1 s_0' b$$

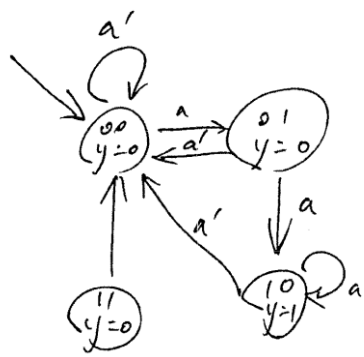
$$y = s_1 \oplus s_0$$

4)

$n_1 = a(s_1 \oplus s_0)$

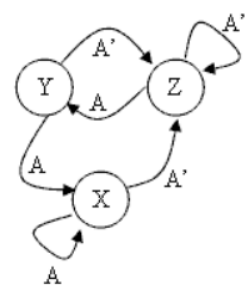
$n_0 = s_1' s_0' a$

$y = s_1 s_0'$



5)

S1	S0	A	D1	D0
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	DC	DC
1	1	1	DC	DC

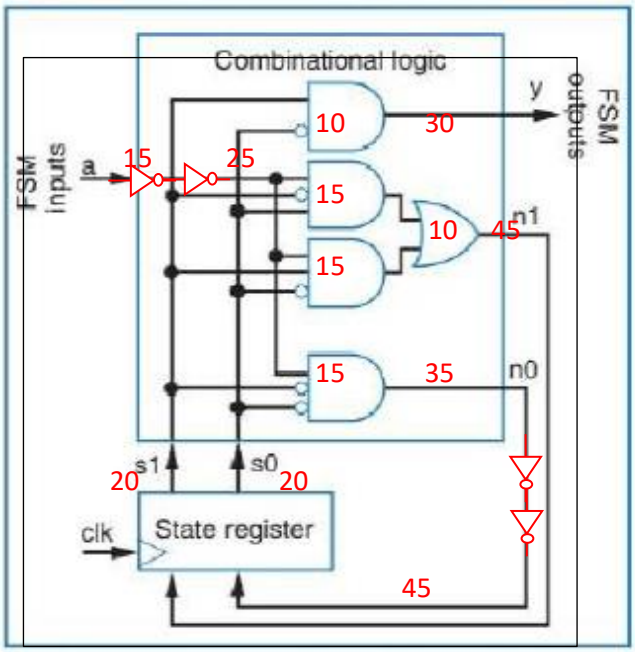


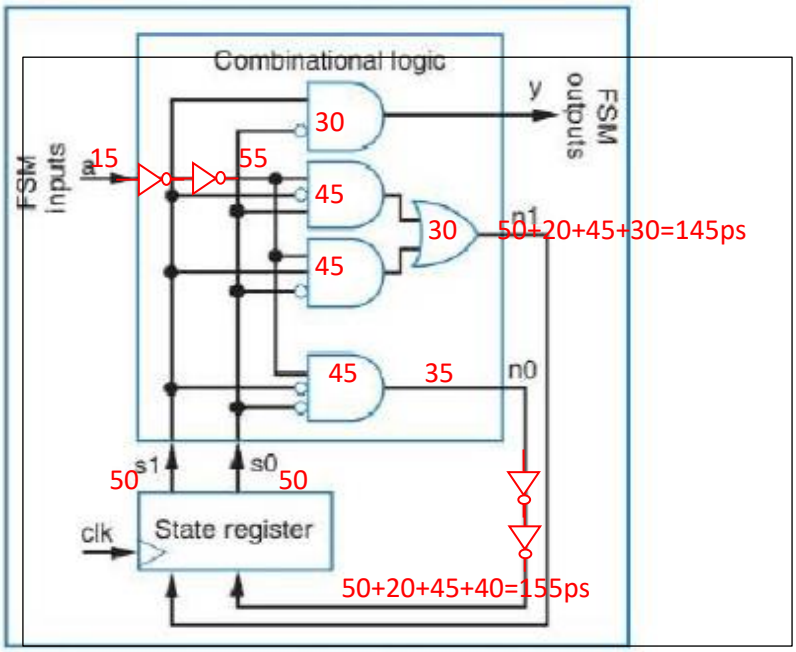
D1=!A

D0=!S1*A

Bob=!S1*!S0

6)





155ps for delay+50ps for setup time=205ps~=4.88GHz