EECS 270 Class Schedule: Fall 2020

#	Date	Topic	Reading	Labs due	Homework
1	Monday, August 31	Class intro, intro to basic logic & logic circuits, binary/hex, MUX	1, 2.4-2.6	**(Tutorial)**	
2	Wednesday, September 02	More on basic logic, combinational logic design	2.7, 2.8, 2.10, 4.3		
	Monday, September 07	**Labor day, No class**		**Lab 1 pre-lab**	
3	Wednesday, September 09	Delay, MSI devices	2.9, 2.10, 4.6	(Due at end of lab period)	**HW1 due**
4	Monday, September 14	Verilog introduction, negative numbers and adders/subtractors	notes, 4.6	**Lab 1, Lab 2 pre-lab**	**GA 1 due**
5	Wednesday, September 16	Logic practice and combinational review (w/ focus on number apps)	2.4-2.10, 3.1-3.2		
6	Monday, September 21	Latches and Flip-flops	3.1-3.3	**Lab 2, Lab 3 pre-lab**	**HW2 due**
7	Wednesday, September 23	More latches and flip-flops, FSM	3.2-3.5		
8	Monday, September 28	More FSM, Seq. Verilog	3.3, 4.2, 4.8	**Lab 3 part 1**	**HW3 due**
9	Wednesday, September 30	Non-ideal issues (set-up, hold and more), sequential verilog	3.3-3.5		
	Monday, October 05	**Exam 1 (In class)**	--	**Lab 3 part 2, Lab 4 pre-lab**	
10	Wednesday, October 07	Memory, logic minimization	5.7, 6.1-6.2		**GA2 due**
11	Monday, October 12	Logic minimization	**6.1-6.2**	**Lab 4**	
12	Wednesday, October 14	Digital design--datapath and control	5		
13	Monday, October 19	Digital design--datapath and control	5	**Lab 5 pre-lab, Lab 5**	**HW4 due**
14	Wednesday, October 21	Digital design--datapath and control	5		
15	Monday, October 26	CMOS design	2.1-2.4	**Lab 6 pre-lab**	**GA3 due**
16	Wednesday, October 28	Sequential logic optimizations (State minimization); K-maps again	6.2-6.3		
17	Monday, November 02	Combinational logic optimization (faster adders)	6.4	**Lab 6**	**HW5 due**
18	Wednesday, November 04	Bus-based datapath design (including a computer)	Notes		
19	Monday, November 09	Combinational logic optimization (Q-M)	6.2, Handout	**Lab 7 pre-lab**	**HW6 due**
	Wednesday, November 11	**Exam 2, covers lec 1-18 (In class)**	----		
20	Monday, November 16	Finish up Q-M	6.2, Handout	**Lab 7 part 1**	
21	Wednesday, November 18	Sequential logic optimization (State encoding, Moore vs. Mealy)	6.3		
23	Monday, November 23	**Thanksgiving**			
24	Wednesday, November 25	**Thanksgiving**			
22	Monday, November 30	TBD/catchup	TBD	**Lab 7 part 2**	**GA4 due**
23	Wednesday, December 02	How logic is built today	2.1-2.4	Fully virtual	
24	Monday, December 07	Exam review		**No lab**	**HW7 due**
	Monday, December 14	**Final exam (1:30-3:30)**			

It's unclear how on-line lectures are going to impact pacing The schedule will be updated as we go.

Notes:

* All lab assignments are due in the first 30 minutes of lab unless otherwise noted.
* Postlabs are due at the same time as the last part of the inlab
* HW is individual homework, GA is a Group Assignment