Schedule for EECS 270, Spring Semester 2022

Date	Week	Topic	Due	Reading	Prelab	Inlab & Postlab
Monday May 02	1	**No class -- Classes start on the 4th**				
Wednesday May 04		Class intro, intro to basic logic & logic circuits, binary/hex, MUX		1, 2.4-2.9		Tutorial
Friday May 06		Combinational logic design, delay, start MSI devices		2.9-2.10, 4.3		1
Monday May 09	2	MSI, 2's complement, adders/subtractors combinational Verilog	HW1	2.10, 4.6	2	
Wednesday May 11		Logic practice, latches and flip-flops	GA1	3.1-3.2	3	2
Friday May 13		Introduce FSMs, develop D flip-flops	Quiz1	3.2-3.3		
Monday May 16	3	More FSM, sequential Verilog	HW2	3.3-3.4		3 part 1
Wednesday May 18		Non-ideal issues (set-up, hold and more), sequential MSI	GA2	2.10, 4.2, 4.8		
Friday May 20		Memory, logic minimization	Quiz2	5.7, 6.1-6.2	4	3 part 2
Monday May 23	4	Finish K-maps, digital design--data path and control	HW3	5, 6.1-6.2		4
Wednesday May 25		Catchup, exam review	GA3		5	
Friday May 27		**Midterm exam (in class)**				
Monday May 30	5	**Memorial Day--no class**				
Wednesday Jun 01		Data path and control (examples)	HW4	5		5
Friday Jun 03		Transistors and CMOS	Quiz3/GA4	2.2-2.3	6	
Monday Jun 06	6	State minimization, faster adders	HW5	4.3, 6.3		
Wednesday Jun 08		Review CLA, bus-based datapath design	GA5	5		6
Friday Jun 10		Bus-based datapath design;	Quiz4	5	7	
Monday Jun 13	7	Mealy machines and QM minimization	HW6	6.3, handout		7 part 1
Wednesday Jun 15		QM example, Mealy machines, errors	GA6	6.3, handout		
Friday Jun 17		Yet more Mealy, how logic is built today	Quiz 5	6.3, handout		
Monday Jun 20	8	Class overview and practice problems.				7 part 2
Thursday Jun 23		Final Exam, 4-6pm				