# EECS 270 Midterm

Spring '05, Prof. Mark Brehob

Name: _____ uname: _____

Sign the honor code:

I have neither given nor received aid on this exam.

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Scores:

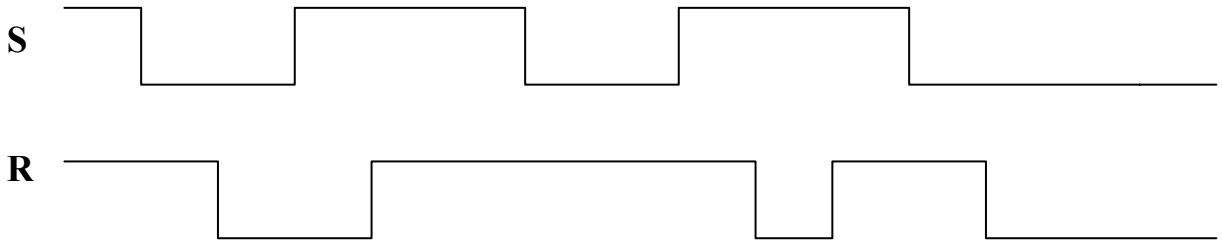
| # | Points |
|---|---|
| 1 | /15 |
| 2 | /15 |
| 3 | /15 |
| 4 | /15 |
| 5 | /20 |
| 6 | /15 |
| 7 | /5 |
| **Total** | **/100** |

**NOTES:**

- This exam will last 120 minutes.
- Throughout this exam * = AND, +=OR, !=NOT $\oplus$ = XOR
- Open book (our text only!), open notes. No computers, cell phones, or other communication devices.

1. Using a K-map find the *minimal product-of-sums* for
   $\Pi_{WXYZ}=(3,4,5,7,9,14,15)+d(10,13)$. Put a star in each of the distinguished one-cells.
   **[15]**

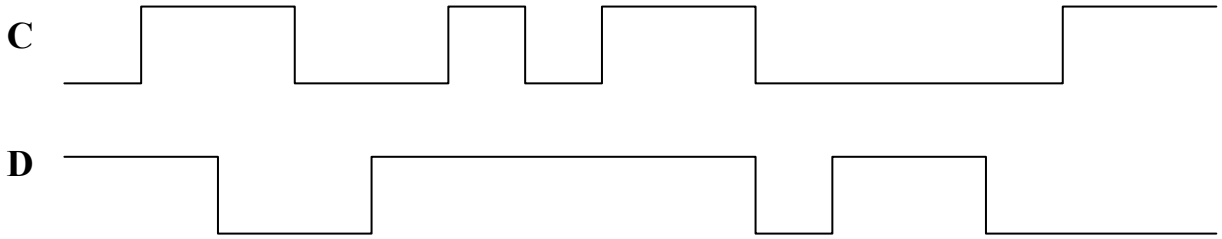
2. Functionality of latches and flip-flops
    a. Show the values of Q and QN for an SR latch with the following inputs. **[9]**




**Q**

**QN**

    b. Show the value of the output of a D-flip-flop given the following input. You should assume the initial value of Q is 0. **[6]**

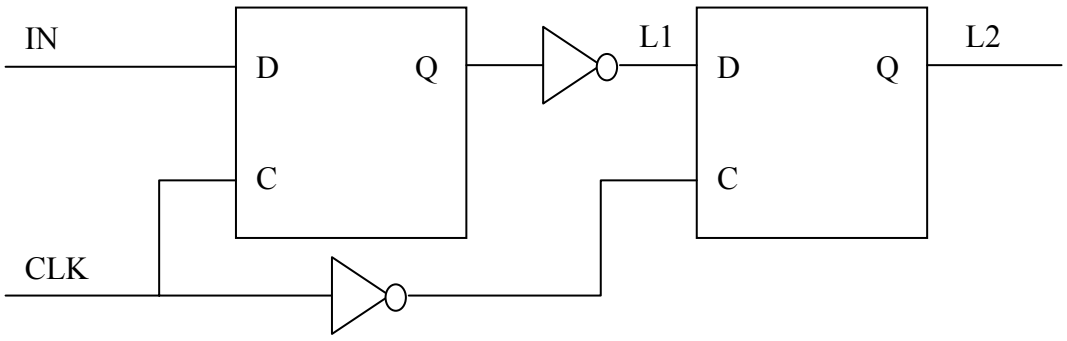



**Q**

3. Find the *minimal sum-of-products* of the following logic equation using the Quine-McCluskey algorithm. You must ***clearly*** show your work for credit, using the algorithm as discussed in class. Solving the problem in some other way will result in 0 points. **[15]**

$$\Sigma_{WXYZ}=(0,1,12,13,15)+d(4,14)$$

4. Analyze the following circuit by showing the values at nodes L1 and L2 at each step. Assume both latches are initially outputting zero. The boxes are D latches. **[15]**




**IN**

**CLK**

**L1**

**L2**

5. Consider a device (named DIFF) which takes two 4 bit *unsigned* numbers as input and outputs a 4 bit unsigned number which is equal to the larger of the two minus the smaller of the two. So for example, if 12 and 4 were the two binary numbers provided as input, the output would be 8.

    a. What would be the output (in binary) if the two inputs were 1000 and 0011? **[2]**

    b. Design a circuit that computes the result of taking the larger minus the smaller value. 4-bit unsigned binary numbers. <u>You should write your solution on the following page</u> and use the notation for the inputs and outputs provided below. A3, B3, and D3 are the most significant bits. You may use: **[18]**
        - AND gates, OR gates, XOR gates as well as NOT gates
        - 4-bit adders (inputs and output are both 4-bits) with carry-in and carry-out.
        - 8 to 3 encoders (all wires active high)
        - 3 to 8 decoders (all wires active high)
        - 4-bit unsigned comparator (all wires active high, has an EQ and GT output)
        - 2 to 1 MUXes (all wires active high)
        - 8 to 4 MUXes (all wires active high)

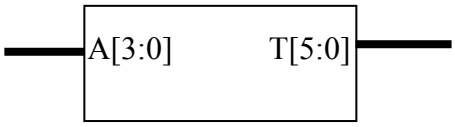
*(This page left blank to give you space for your answer to the previous problem)*

6. Consider a device that takes as input a 4-bit 2's complement number and outputs a 6-bit 2's complement number that is equal to twice the input value. So if the input were –1 as a 4-bit 2's complement number, the output should be –2 as a 6-bit 2's complement number.
    a. If the input were 0010 what should the output be (in binary)? **[2]**

    b. If the input were 0110 what should the output be (in binary)? **[2]**

    c. If the input were 1010 what should the output be (in binary)? **[2]**

    d. Using only AND, OR, NOT, and XOR gates, design a circuit which implements the above function. Use the naming convention found in the figure below. A3 and T5 are the most significant bits. **[9]**



7. If the 74x153 has the following input values:
   - A, 1G, 1C0, 1C2, 2G and 2C1 are all zero
   - All other inputs are one

   What is the value of 1Y and 2Y? **[5]**