EECS 270 *Midterm Exam*

Spring 2014

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

_____

Scores:

Problem #	**Points**
1	/12
2	/5
3	/6
4	/11
5	/10
6	/10
7	/13
8	/15
9	/18
Total	**/100**

NOTES:

1. Open book and Open notes
2. There are 11 pages total. Count them to be sure you have them all.
3. No electronic devices of any kind are allowed on this exam.
4. This exam is fairly long: *don't spend too much time on any one problem*.
5. You have about 120 minutes for the exam.
6. Some questions may be more difficult than others. You may want to skip around.
7. **Be sure to show work and explain what you've done when asked to do so.** Even if work isn't requested it is a good idea to provide your work as it will help with partial credit.

1) Fill in each blank or circle the best answer.**[12 points, -2 per wrong or blank answer, min 0]**

   a) 100011, when treated as a 6-bit two's complement number, has a decimal representation of

      _____.

   b) The 6-bit signed-magnitude representation of -9 is _____.

   c) A clock period of 10ns corresponds to a frequency of _____GHz.

   d) Consider a memory device that has 1024 addresses each 16 bits in size. If this was made out of a square memory (equal number of rows and columns in the memory device) the row

      decoder would have _____inputs while the column MUX would have

      _____ selection bits.

   e) The *canonical* sum-of-products representation of (A+B)*!C is: _____

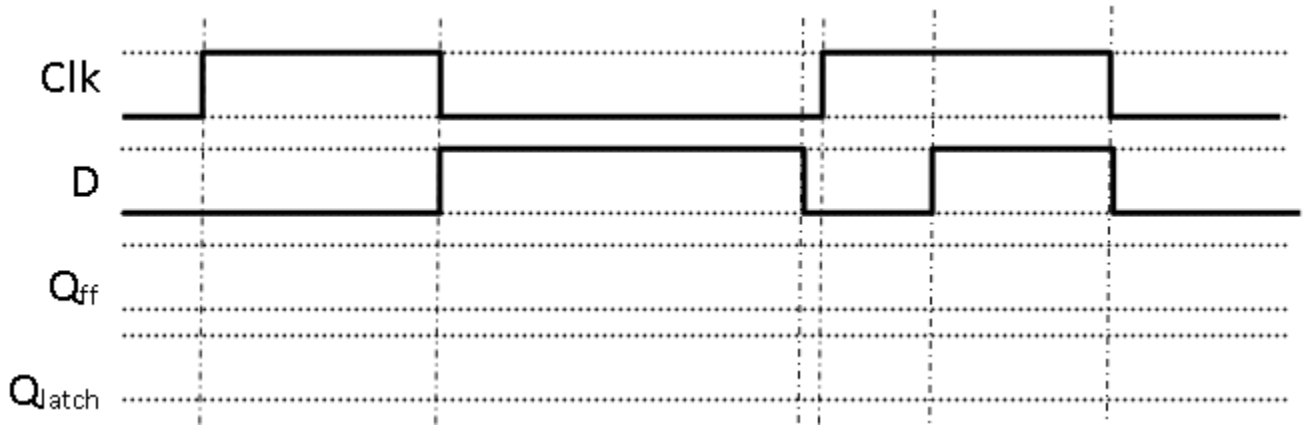
   f) An 8 to 3 priority encoder has would have an output of O[2:0]= _____ (in binary) if the input were 8'd12.

   g) ***DRAM / SRAM / Neither DRAM nor SRAM / Both DRAM and SRAM*** generally uses a capacitor to store the value of a cell.

   h) 31.03_5 is _____ as a decimal number.

2) Using only a decoder and an OR gate (of any number of inputs) create a circuit which implements the following logic F= (A+B)*(A+C')*(A+B'+C)
   [5 points]

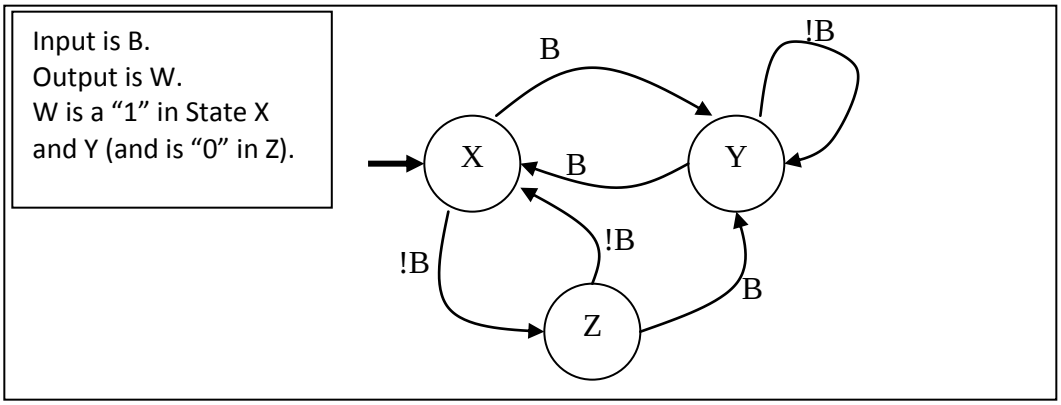
3) Complete the timing diagram for a D flip-flop and a D latch. You may assume that the setup and hold times are infinitesimal and that two events are simultaneous if and only if they share the same dotted line. **[6 points]**



4) Draw the state transition diagram which is implemented by the Verilog found below. You should only include states that can be reached from the initial (reset) state. *Clearly show your work.* **[11 points]**

```
module SM1 (clock, reset, A, B, X);

input clock, reset, A, B;
output X;
reg  [1:0] state;
wire [1:0] next_state;

always @ (posedge clock)
begin
 if (reset == 1'b1)
  state <= 2'b00;
 else
  state <= next_state;
end // end of always @ (posedge clock)

assign next_state[0] = !state[1]&A | state[1]&A&B | state[0];
assign next_state[1] = !state[1]&!state[0]&!A | state[1]&!(A&B);
assign X             = state[0];

endmodule;
```

5) Design a state machine which implements the following state transition diagram. Assign state bits S[1:0] as 10 for state X, 01 for state Y, and 11 for state Z. You are to assume that you will never reach the state S[1:0]=00, so you don't care what happens in that case. You must show your work to get any credit! *You only need to compute the next state and output logic, you don't need to draw the gates or flip-flops!* Place your answer where shown, ***all answers must be in product-of-sums form***. **[10 points]**



*(Be sure all are in **product-of-sums** form!)*

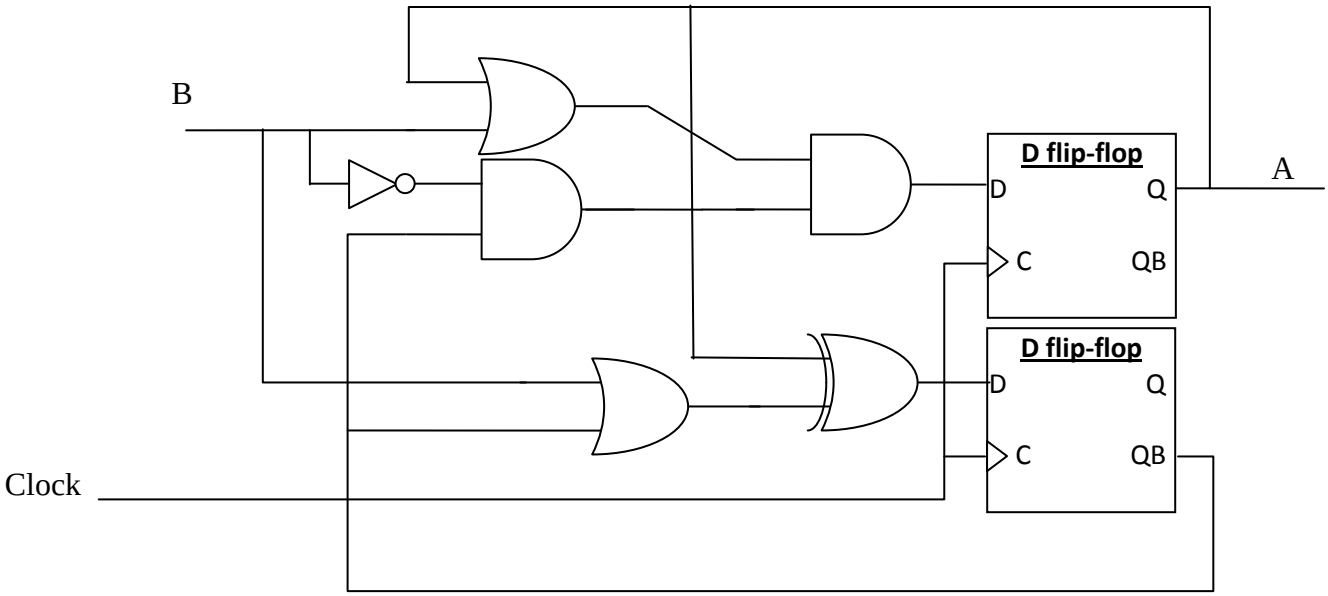
NS1= _____

NS0= _____

W= _____

	Min	Max
OR/AND	3ns	5ns
NOT	1ns	2ns
XNOR	2ns	8ns

DFF:		**Min**	**Max**
	Clock to Q	2ns	4ns
	Set-up time	3 ns	
	Hold time	???? ns	



6) Assuming "B" is coming from a flip-flop with the same characteristics as those listed above, answer the following questions **[10 points]**
   a) In order for this circuit to work correctly, what range of values that would be acceptable for the hold time *requirement* of the D flip-flops? Assume the only options range from 1ns to 10ns. Clearly show your work. **[5]**

      Smallest _____ Largest _____

   b) What is the highest clock *frequency* that could be safely used on this circuit? Clearly show your work. **[5]**

7) Consider a device that takes two unsigned 4-bit numbers as inputs and generates the *average* of these to values as an unsigned 4-bit number. **[13 points]**
   a) What would be the *sum* of the binary values 1010 and 0100? Provide your answer in binary. **[1]**

   b) What would be the *average* of the binary values 1010 and 0100? Again, provide your answer in binary. **[1]**

   c) What would be the sum and average of 1001 and 1111? **[1]**

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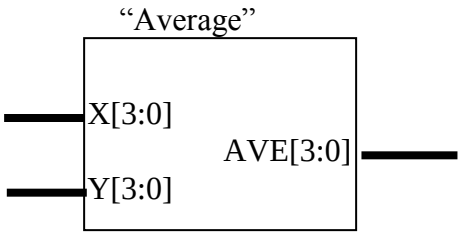
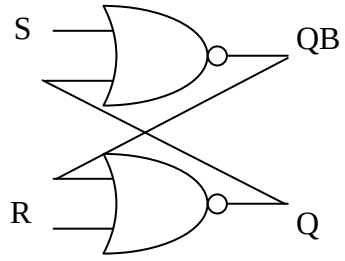
d) Design a circuit that computes the *average* of two 4-bit unsigned binary numbers. If the average is not a whole number, you may round up or down (your choice) but you must either always round up or always round down. Inputs and outputs are as shown below. Your answer will be graded in part for clarity (it is clear what is going on) and simplicity (you don't use unneeded components). **[10 points]**

You may freely use:

- AND gates, OR gates, XOR gates, NOT gates, "0s" (ground) and "1s" (power)
- 4-bit adders (inputs and output are both 4-bits) with carry-in and carry-out.
- 16 to 4 encoders
- 4 to 16 decoders
- 4-bit unsigned comparator (has an EQUAL and GREATER output)
- 2 to 1 MUXes
- 8 to 4 MUXes



8) Below is diagram and a truth table for an SR-latch. Using similar notation, write the truth table for the device pictured below. Answer the following questions: **[15 points]**



S	R	Q	QB
0	0	lastQ	lastQB
0	1	0	1
1	0	1	0
1	1	0	0

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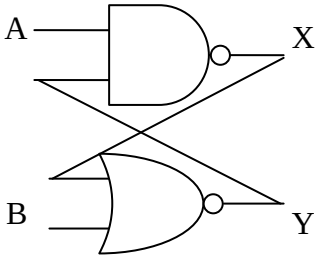
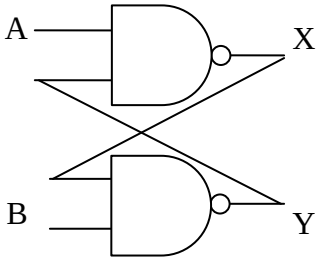
a) Using the SR latch as a template, complete the truth table for the device below **[5, -1 per wrong or blank table entry, minimum 0]**



A	B	X	Y
0	0		
0	1		
1	0		
1	1		

b) Again using the SR latch as a template, complete the truth table for the device below **[5, -1 per wrong or blank table entry, minimum 0]**



A	B	X	Y
0	0		
0	1		
1	0		
1	1		

c) Consider the two devices drawn above. Which of the above can be used as a latch? Your answer should be either "a", "b", "both" or "neither". Justify your answer. **[5]**

9) Draw a state transition diagram for a state machine that takes two inputs "A" and "B" and generates an output X. You will lose points for inefficient designs. **[18 points]**

a) Output X is a 1 if, and only if, A>B thus far where A and B are treated as *signed-magnitude numbers*, MSB first. **[9]**

For example if **A=11001100** [A is 0, -1, -2, -4, -9, -19, -38, and -76]
B=11100110 [B is 0, -1, -3, -6, -12, -25, -51, and -102]
Then **X=00111111**

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b) Output X is a 1 if, and only if, A>B thus far where A and B are treated *as signed-magnitude numbers*, LSB first. **[9]**

For example if **A=11001100** [A is 0, -1, 3, 3, -3, -19, 19, and 19]
B=11100110 [B is 0, -1, -3, 7, 7, -7, -39, and 103]
Then **X=00100010**