EECS 270 *Midterm 1 Exam* Closed book portion

Spring 2022

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

_____

NOTES:

1. ***This part of the exam is closed everything. No calculators, books, notes, etc.***
2. Once you finish this part, turn it in and you'll be given the open book part. You won't be able to come back to this part.
3. There are 3 pages total. Count them to be sure you have them all.
4. You have about 120 minutes for the exam total. We'd suggest you not spend more than 25 minutes or so on this part.
5. In this document we use * for AND, + for OR, ! for NOT, and $\oplus$ for XOR.

1. Using only inverters and tri-state buffers, implement an XNOR gate with inputs A, B and an output X. You may use no more than 4 devices total. **[4 points]**

2. Fill in each blank.**[8 points, -1.5 per wrong or blank question, min 0]**

   a) The 5-bit 2's complement number representation of -4 is _____.

   b) The range of representation for a 4-bit signed-magnitude number is from _____ to _____.

   c) The number 22.3_8 is _____ in base 16.

   d) If a clock has a frequency of 500MHz, it has a period of _____ns

   e) The canonical sum-of-products representation of (A+B) is _____

   f) The canonical product-of-sums representation of !(A*B) is _____

3. Prove some version of De Morgan's law by using perfect induction. **[3]**

4. Complete the following timing diagram for an SR-latch with enable. You may assume that the time scale is such that the gate delay is extremely small and your answer should not reflect those delays. Changes shown to be simultaneous are exactly simultaneous. **[5 points]**

   If the value is unknown (or oscillating or metastable) at some point, clearly indicate that with hashes (like this)