EECS 270 *Midterm 1 Exam* Closed book portion

Winter 2017

Name: _____ unique name: _____

Sign the honor code:

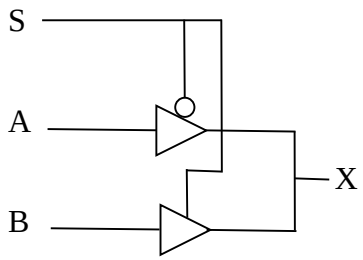
I have neither given nor received aid on this exam nor observed anyone else doing so.

_____

NOTES:

1. ***<u>This part of the exam is closed everything. No calculators, books, notes, etc.</u>***
2. Once you finish this part, turn it in and you'll be given the open book part. You won't be able to come back to this part.
3. There are 3 pages total. Count them to be sure you have them all.
4. You have about 120 minutes for the exam total. We'd suggest you not spend more than 25 minutes or so on this part.
5. In this document we use * for AND, + for OR, ! for NOT, and $\oplus$ for XOR.

1. Using only inverters and tri-state buffers, implement a 2-to-1 MUX with inputs A, B, and S as well as an output X. If S=0, X should equal A. If S=1 X should equal B. You may use no more than 4 devices total. **[4 points]**



2. Fill in each blank or circle the best answer.**[13 points, -2 per wrong or blank question, min 0]**

   a) With a D-flip-flop, there is a short period before the rising edge of the clock where the D input must remain constant or the flip-flop may not behave correctly. That short time is called the

   _____setup_____ time.

   b) The 5-bit 2's complement number representation of -3 is ____11101_____.

   c) The range of representation for a 6-bit signed-magnitude number is from _-31__ to _31___.

   d) If a clock has a frequency of 50MHz, it has a period of _____20_____ns

   e) The canonical sum-of-products representation of (A⊕B) is _____!AB + A!B_____

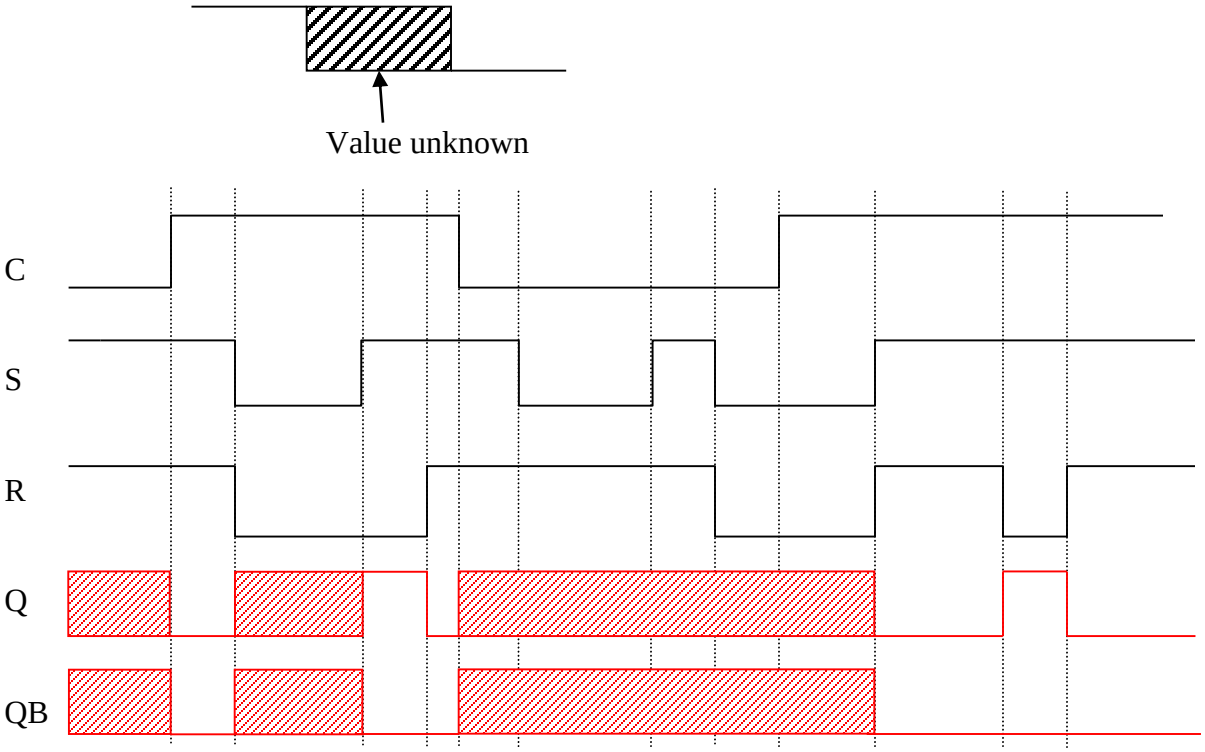
   f) The canonical product-of-sums representation of (A⊕B) is _____(A+B)(!A+!B)_____

   g) That (A*B) = (B*A) is an example of the _____commutative_____ property of logic.

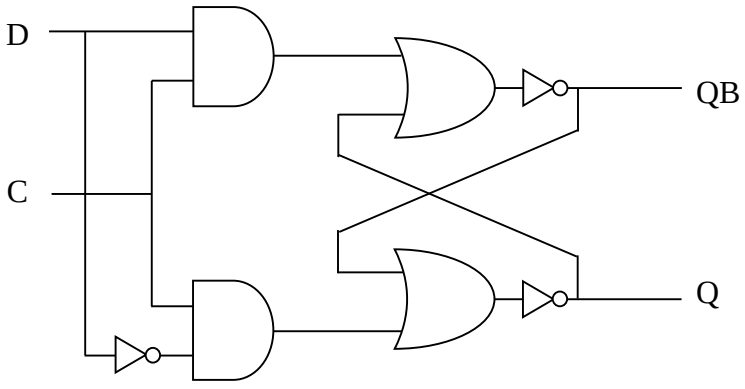
   h) The number 231_{16} is _____1061_____ in base 8.

3. Complete the following timing diagram for an SR-latch with enable. You may assume that the time scale is such that the gate delay is extremely small and your answer should not reflect those delays. Changes shown to be simultaneous are exactly simultaneous. **[6 points]**

   If the value is unknown (or oscillating or metastable) at some point, clearly indicate that with hashes (like this)



4. Implement a D-latch using *only AND, OR and NOT* gates (no bubbles, NOR gates, or NAND gates). Clearly label your inputs (D, C) and outputs (Q, QB). There will little or no partial credit for this question. **[4 points]**



EECS 270 *Midterm 1 Exam* Open book portion

Winter 2017

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_____

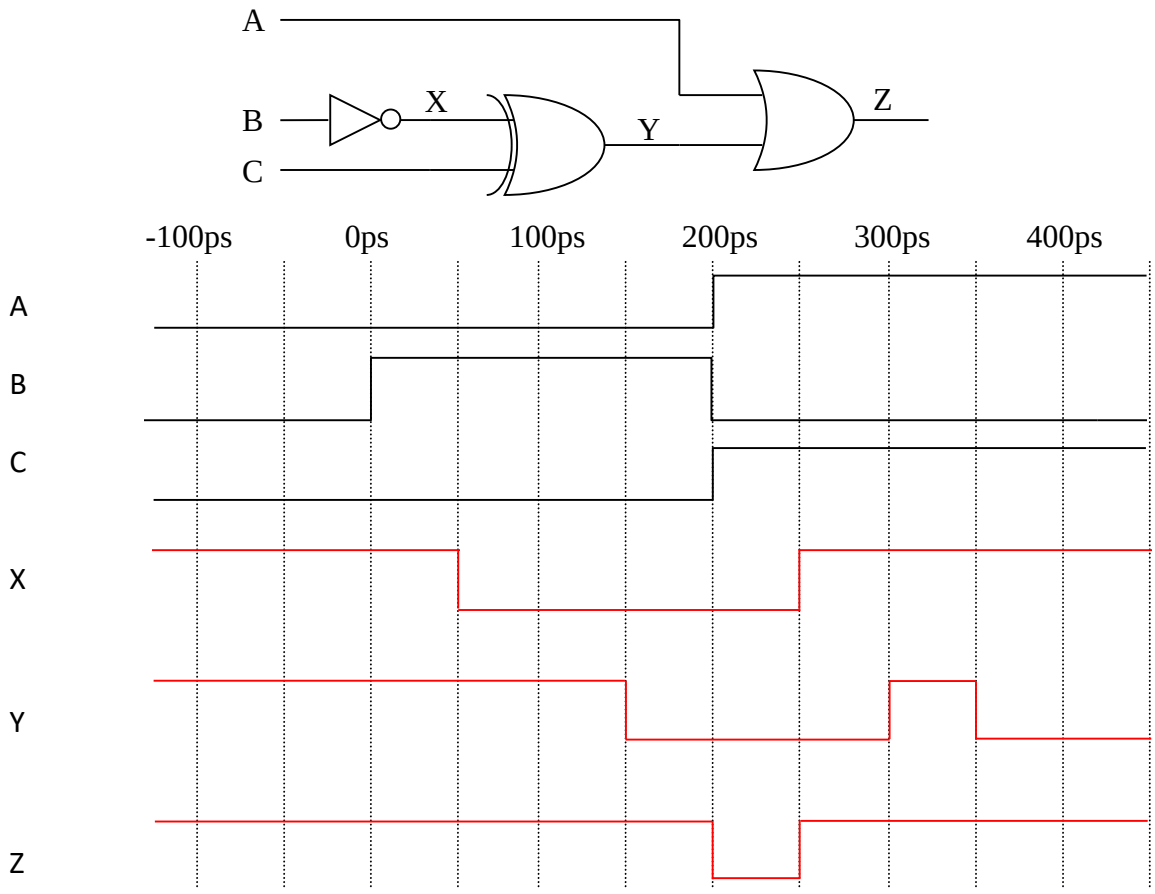
NOTES:

1. ***<u>This part of the exam is open books and open notes. You may not use any device capable of communication (cell phones, calculators with wireless, etc.)</u>***
2. You have about 120 minutes for the exam total.
3. Some questions may be harder than others. Manage your time wisely.
4. Unnecessarily complex designs will likely not get full credit.
5. Be sure to show your work when asked.

1) Using the rules of logic, show that (a*b)+!(!a+d) = a*!(!b*d). You must show each step and clearly identify each rule used. **[5 points]**

(a*b)+!(!a+d)	
(a*b)+(a*!d)	DeMorgan's Law
a(b+!d)	Distributive Property
a!!(b+!d)	Involution
a!(!b*d)	DeMorgan's Law

2) Assuming that NOT and OR gates have a delay of 50ps while XOR gates have a delay of 100ps, complete the following timing diagram from time 0 to 450ps. Assume the inputs have been constant for a long time before 0ps. **[6 points]**



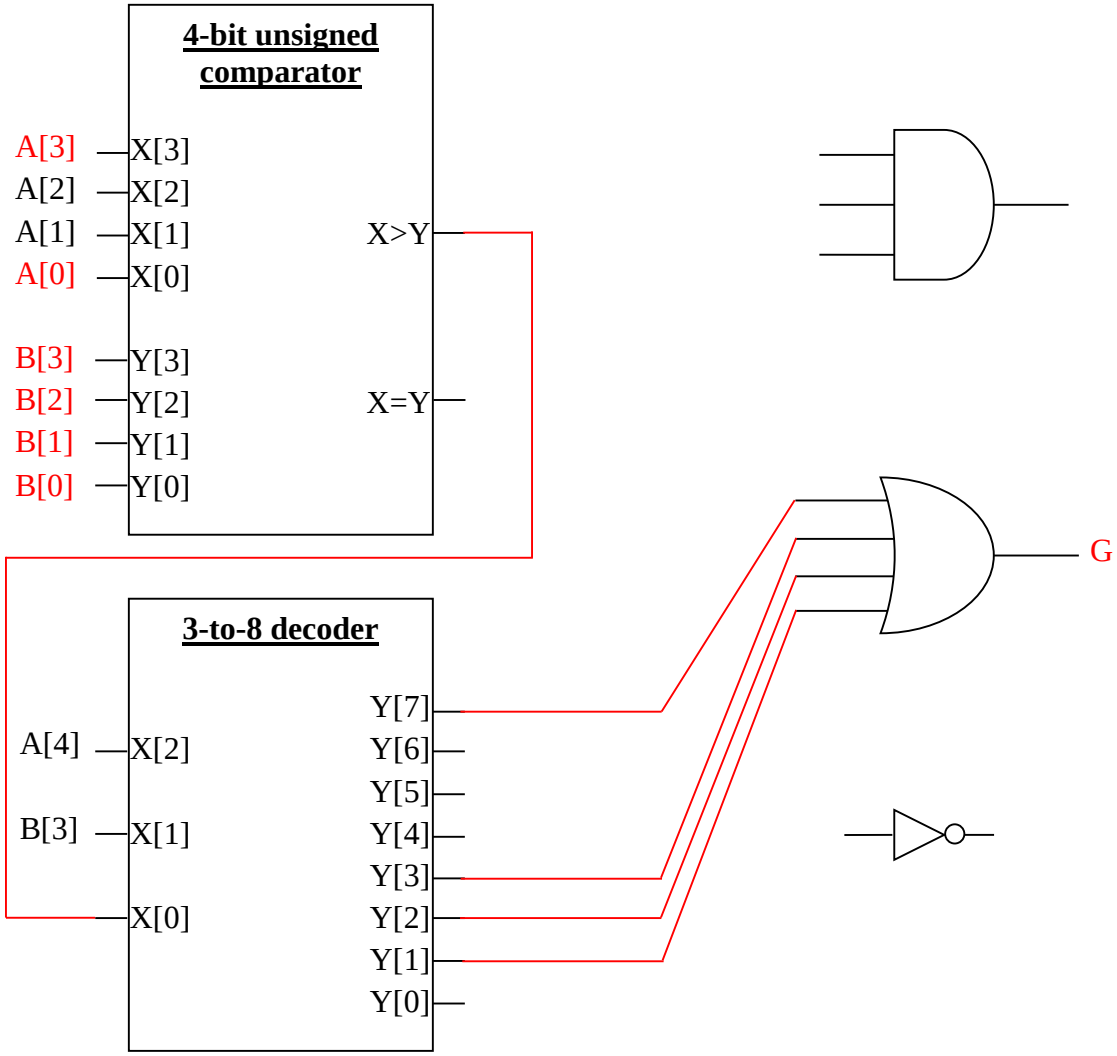
3) The digital design company "Care-less Designers" have hired you to fix a part which someone had dropped and most of wires had fallen out of the board (when you use a breadboard for design, that can actually happen).

The device takes inputs A[4:0] and B[3:0] and is supposed to generate an output G. A and B are 2's complement numbers (5 bits for A, 4 bits for B). G should be a 1 if A>B, otherwise it should be a 0.

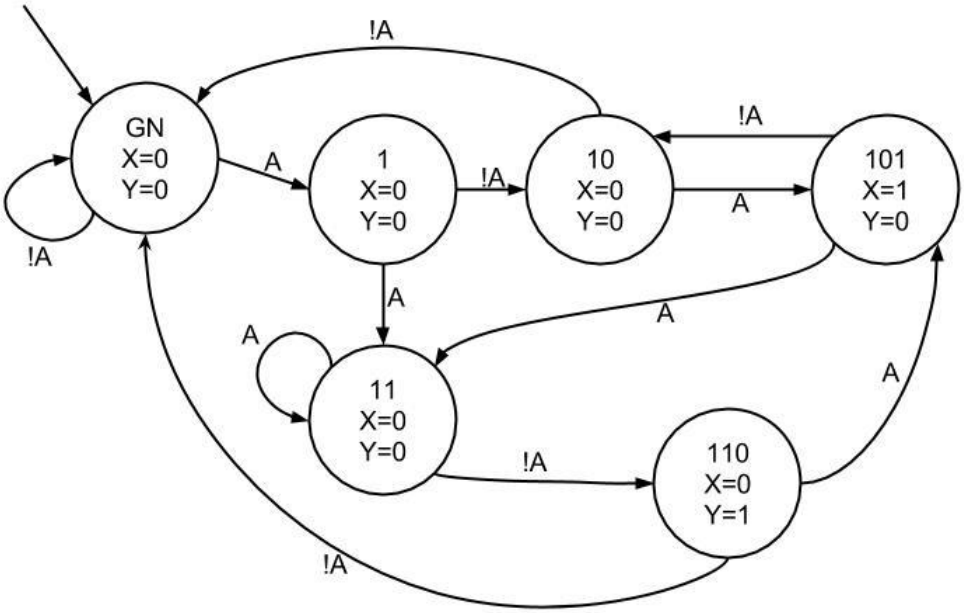
Examples:

- If A=11110 (-2) and B=1111 (-1) then G should be 0.
- If A=00000 and B= 1001 then G should be 1.
- If A=01111 and B=0111 then G should be 1.

Complete the following design. You may add wires as needed (including putting inputs where needed) but may not change anything else. There may be components on the board you don't need to use. You may freely use "1" (power) and "0" (ground) in your design. *Be sure to include the output (G).* **[10 points]**



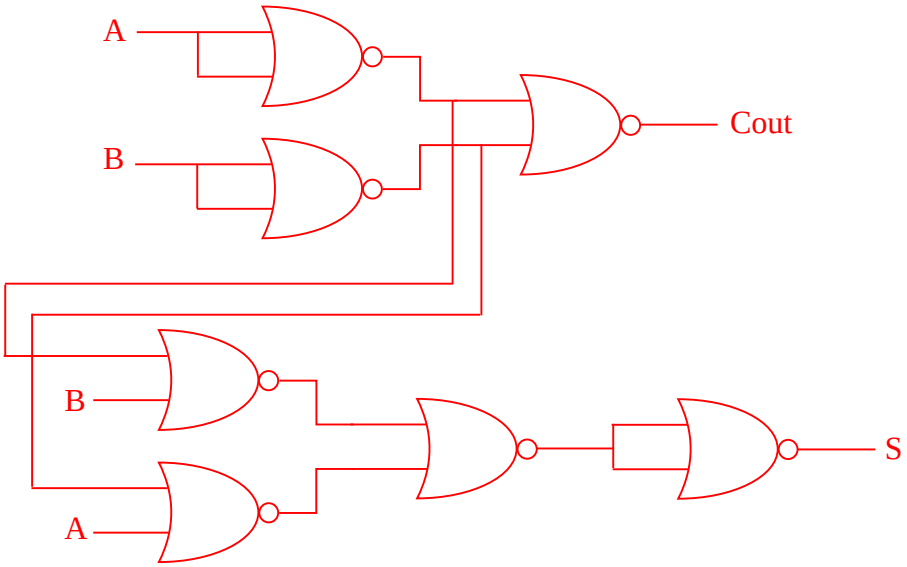
4) Design a state transition diagram for a state machine that takes one input, “A” and generates two outputs “X” and “Y”. X should be a 1 if and only if the most recent values of A have been “101”, Y should be a 1 if and only if the most recent values of A have been “110”. **[10 points]**



5) Design a half-adder (inputs: A, B, outputs: S and Cout) using only 2-input NOR gates. For full credit, you must use 12 or fewer gates. **[9 points]**

Cout = A*B = !!(A*B) = **!(!A+!B)**

S = A*!B + !A*B = !!(A*!B) + !!(!A*B) = **!(!A+B) + !(A+!B)**

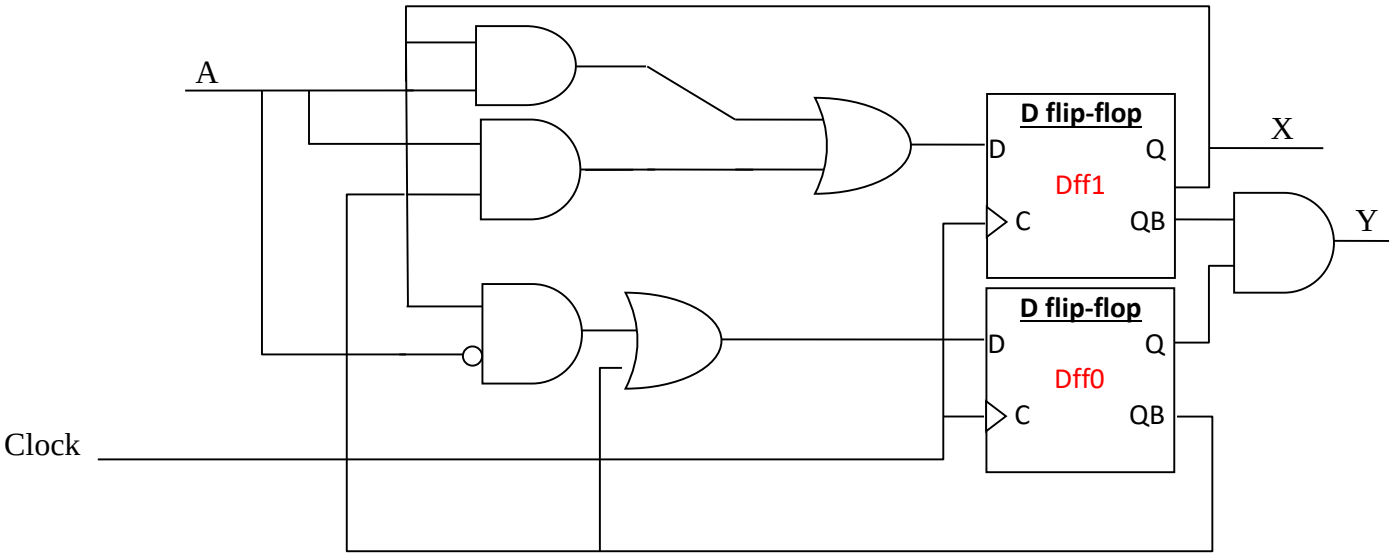


6) How many literals are there in the *canonical* ***product-of-sums*** of the following functions? **[5 points, -2 per wrong or blank answer, minimum 0]**

a. A 2-input NOR gate: _____6_____

b. The sum output of a full adder: _____12_____

c. A 3-input AND gate: _____21_____

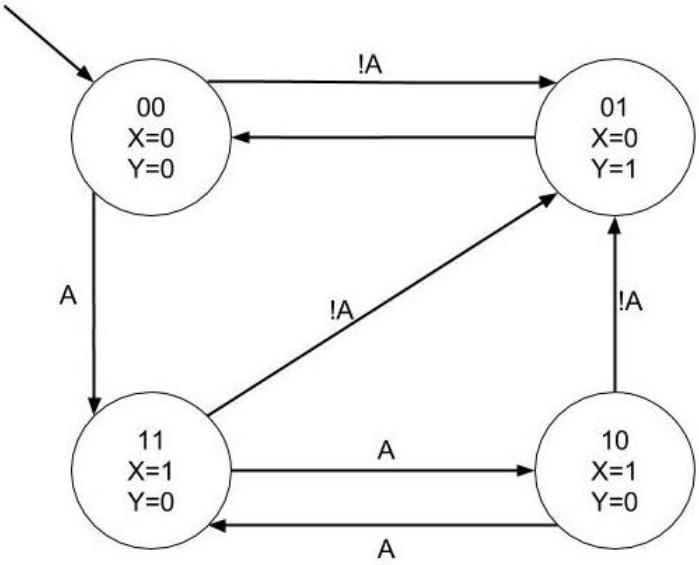


7) Draw the state transition diagram which is implemented by the above circuit. You should assume the initial state is when both flip-flops are "0". You should only include states that can be reached from the initial state. *Clearly show your work.* **[10 points]**

Assuming the top Dff is Q_1 and the bottom as Q_0

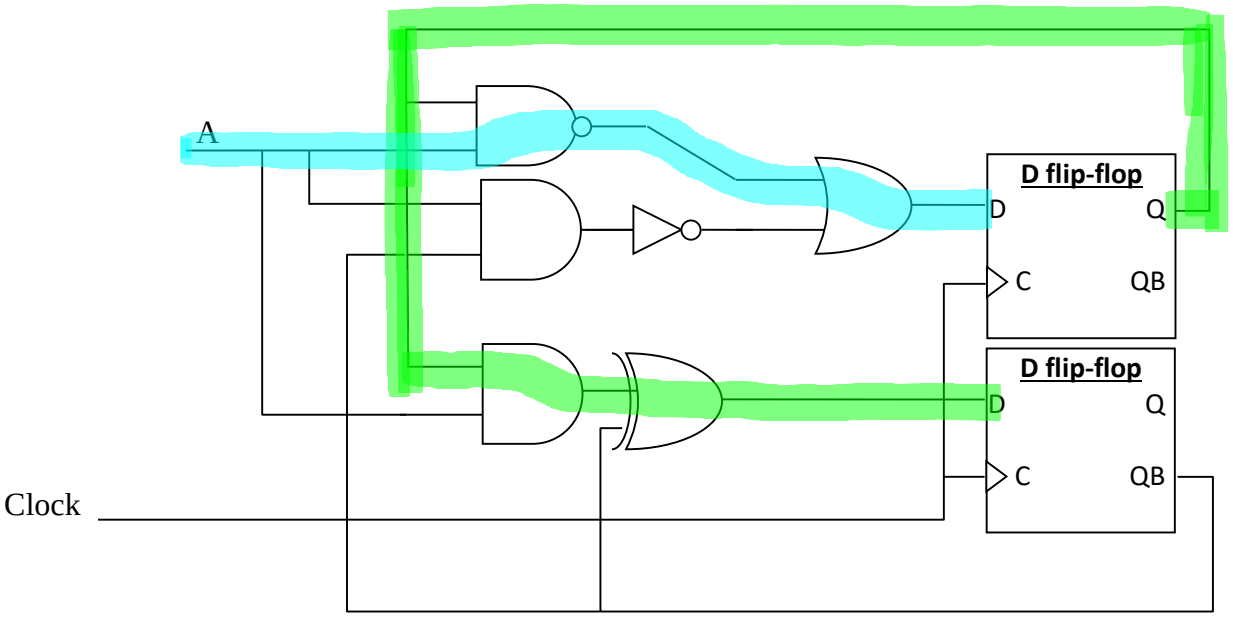
$D1 = AQ_1+A!Q_0$ $\quad X = Q_1$

$D0 = Q_1!A+!Q_0$ $\quad Y = !Q_1Q_0$



	Min	Max
OR/AND	2ns	5ns
NOR/NAND	1ns	4ns
NOT	1ns	1ns
XOR	3ns	9ns

DFF:		**Min**	**Max**
	Clock to Q	2ns	3ns
	Set-up time	7 ns	
	Hold time	??? ns	



8) Assuming the input A *always* arrives 1ns after the rising edge of the clock, answer the following questions. **[10 points]**

- In order for this circuit to work correctly, what range of values that would be acceptable for the hold time *requirement* of the D flip-flops? Assume the only options range from 1ns to 20ns. Clearly show your work. **[4]**

  Smallest _____1ns_____ Largest ____4ns_____

  Fast path highlighted in blue

- What is the lowest clock period that could be safely used to clock this circuit? Clearly show your work. **[6]**
  Slow path highlighted in green

  Clk-to-Q + CLD + Set-Up =
  3ns + 14ns + 7ns = 24ns

9) In class we've designed a state transition diagram serial comparators (lecture 7 notes on page 3). First we did MSB (most significant bit) and later LSB first (least significant bit). This time we are going to compute the *sum* of two numbers, where the numbers are provided one bit at a time, LSB first. You are to design a state transition diagram that has two inputs X and Y, and one output S. S should be what the sum bits would be in a ripple-carry adder if X and Y were the inputs (again, with LSB first). For example:

```
X:010110                    Which is basically
Y:110110                      011010 (X)
S:101011                     +011011 (Y)
                             ========
                              110101 (S)
```

Provide the state diagram that implements this serial adder. **[8 points]**

The state name in quotations signify the carry and sum bits in that state