

EECS 270 Midterm 2 Exam Closed book portion

Fall 2014

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

Scores:

Page #	Points
2	/14
3	/10
<i>Total closed book</i>	<i>/24</i>
<i>Total open book</i>	<i>/76</i>
Total	/100

NOTES:

1. ***This part of the exam is closed everything. No calculators, books, notes, etc.***
2. Once you finish this part, turn it in and you'll be given the open book part. You won't be able to come back to this part.
3. There are 3 pages total. Count them to be sure you have them all.
4. You have about 120 minutes for the exam total. We'd suggest you not spend more than 25 or 30 minutes on this part.

1. Fill in each blank or circle the best answer. [10 points, -2 per wrong or blank answer, min 0]

a) $!(A+B)$, when expanded into canonical sum-of-products form, has _____ minterms.

b) A 4-bit 8 to 1 MUX would require _____ select lines.

c) You are treating the 8-bit numbers A[7:0] and B[7:0] as unsigned numbers. If you set

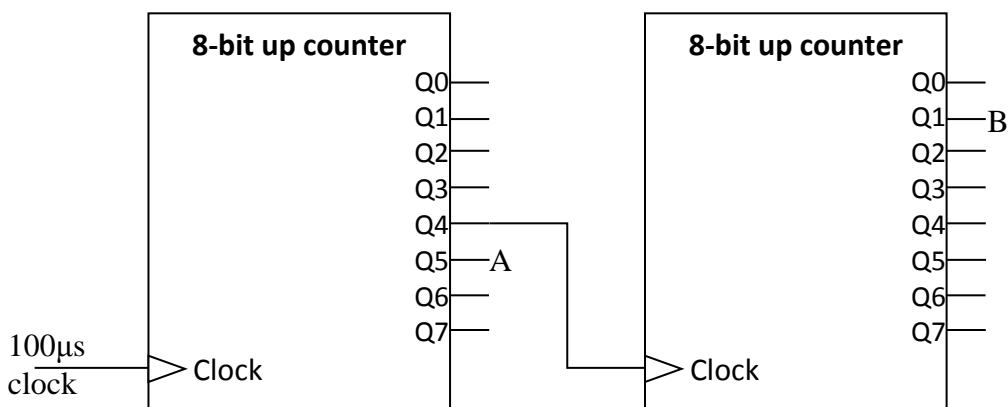
$B[3:0]=A[3:0]$ and $B[7:4]=4'b0000$,

B is now equal to A plus / minus / times / modulo / divided by 2 / 3 / 4 / 8 / 16 / 32

d) When building a 1024 by 4 memory out of a square memory of minimum size, the row decoder will have _____ bits of input while the column MUX will have _____ bits needed for its select input.

e) In CMOS you'd need at least _____ transistors to implement a 4-input OR gate.

2. Two 8-bit counters are connected as follows. Assume that these two counters are both working as "counting up" (note that Q7 is the MSB for the output of a counter); also, the period of the input clock signal for the 1st counter (the one on the left-hand side) is equal to 100 μ s. Calculate the period of the output signals at A and B, respectively. Your answer must be in ms! [4]

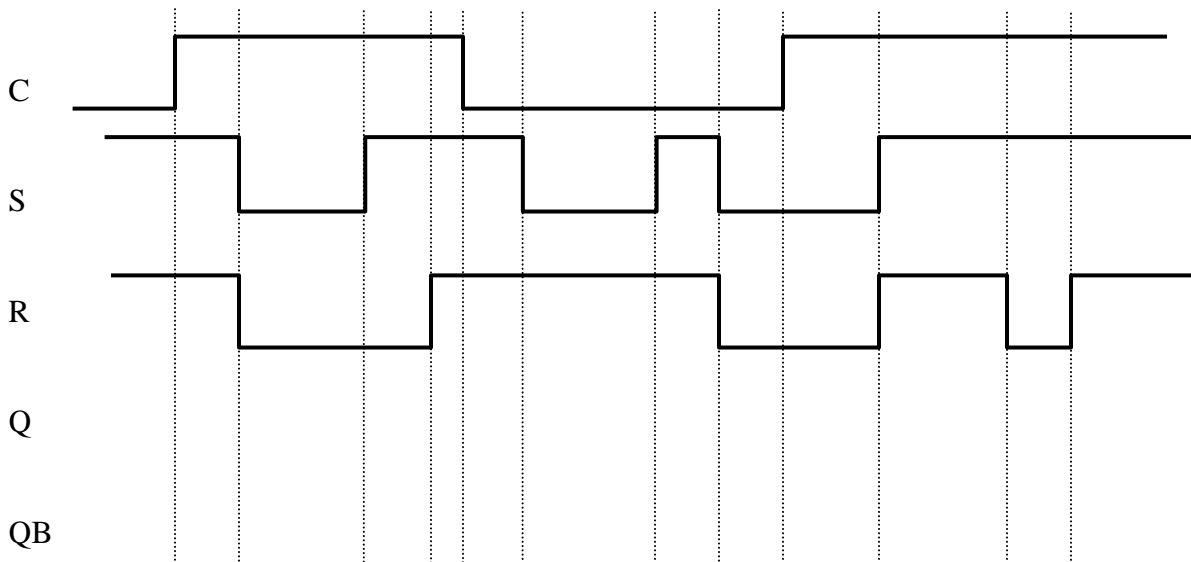
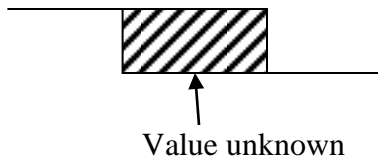


Period of A: _____ms

Period of B: _____ms

3. Complete the following timing diagram for an SR-latch with enable. You may assume that the time scale is such that the gate delay is extremely small and your answer should not reflect those delays. Changes shown to be simultaneous are exactly simultaneous. [5 points]

If the value is unknown (or oscillating) at some point, clearly indicate that with hashes (like this)



4. Find the minimal sum-of-products using this Kmap. Clearly show your work. [5]

		CD			
	AB	00	01	11	10
00	d	1	0	1	
01	0	1	1	1	
11	1	d	d	0	
10	1	d	0	1	

Minimal SoP:

EECS 270 Midterm 2 Exam Open book portion

Fall 2014

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

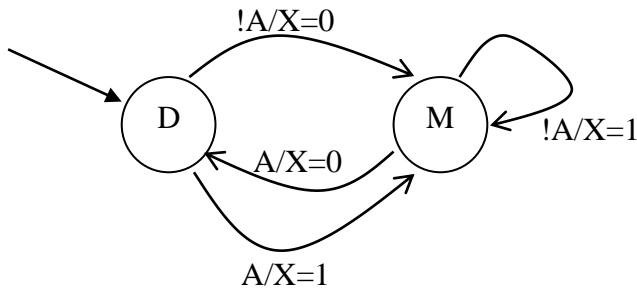
Scores:

Page #	Points
5	/12
6	/12
7	/8
8	/15
9	/15
10	/14
<i>Total open book</i>	<i>/76</i>

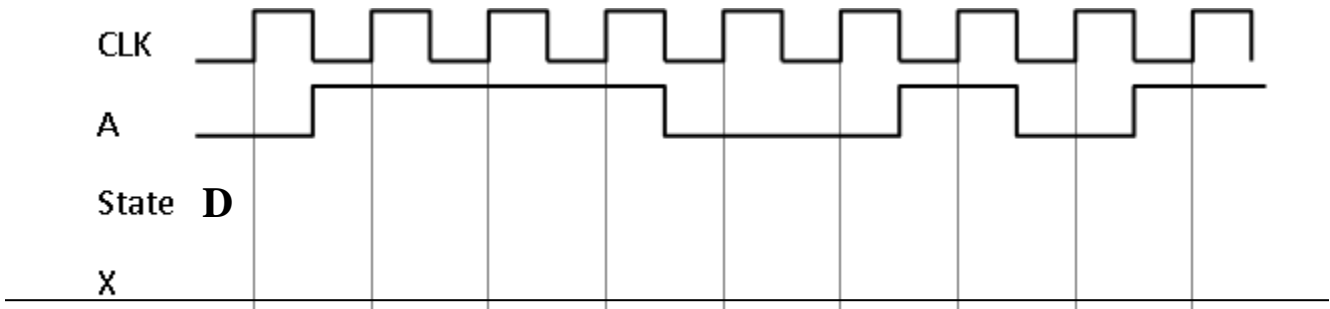
NOTES:

1. *This part of the exam is open books and open notes. You may not use any device capable of communication (cell phones, calculators with wireless, etc.)*
2. You have about 120 minutes for the exam total.
3. Some questions may be harder than others. Manage your time wisely.
4. The last two questions are fairly difficult and potentially time consuming. We recommend you do the rest of the exam before starting those.

1. Consider the following Mealy state transition diagram.

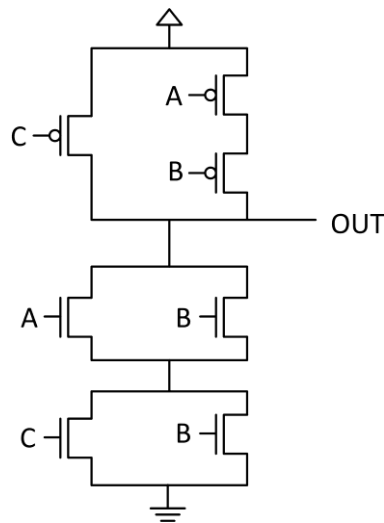


Complete the following timing diagram. . [6 points]



2. Consider the transistor diagram below. Fill in the truth table with either “1”, “0”, “Hi-Z” or “Smoke” (the last if OUT is connected to both Vcc and Ground). [6 points]

A	B	C	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



3. The following table describes a state machine.

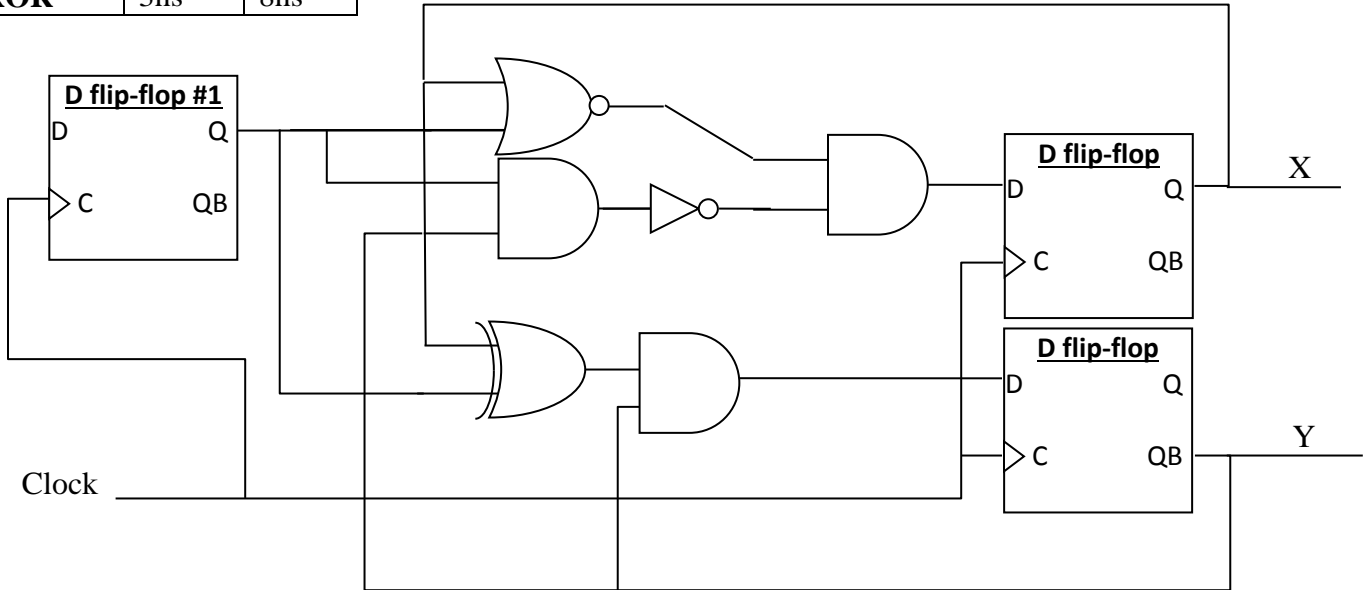
Present state	Next state		Output Z
	x=0	x=1	
A	B	C	0
B	D	E	0
C	F	G	0
D	A	A	0
E	A	A	1
F	A	A	0
G	A	A	1

Minimize the number of states in this machine and *draw* the state transition diagram which describes this minimized machine. Show your work. **[12 points]**

A						
B						
C						
D						
E						
F						
	G	A	B	C	D	E

	Min	Max
AND	???	???
NOR	2ns	5ns
NOT	2ns	3ns
XOR	3ns	8ns

DFF:		Min	Max
	<i>Clock to Q</i>	2ns	3ns
	<i>Set-up time</i>	3 ns	
	<i>Hold time</i>	5 ns	



4. Answer the following questions. Assume we are clocking this circuit at 50MHz. [8 points]

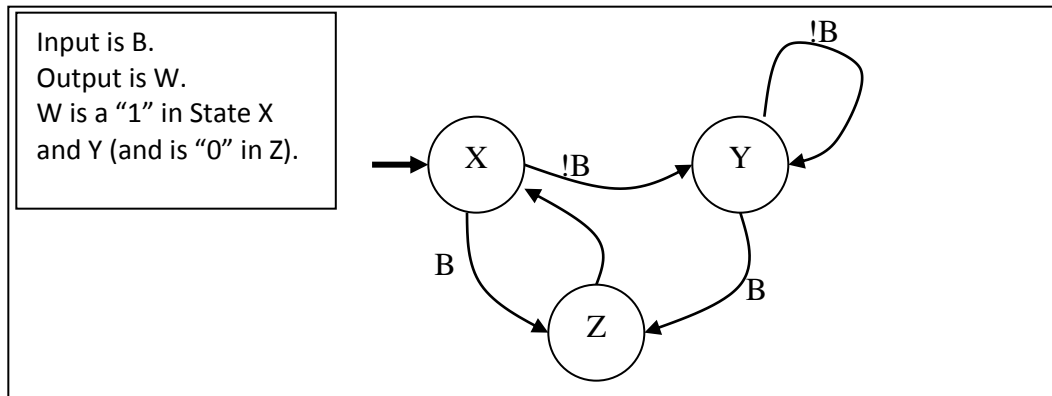
- a) In order for this circuit to work correctly, what range of values that would be acceptable for the minimum time delay of the AND gates? Assume the only options are integers from 1ns to 20ns. Clearly show your work. [4]

Smallest _____ Largest _____

- b) In order for this circuit to work correctly, what range of values that would be acceptable for the maximum time delay of the AND gates? Assume the only options range from 1ns to 10ns. Clearly show your work. [4]

Smallest _____ Largest _____

5. Design a state machine which implements the following state transition diagram. Assign state bits $S[1:0]$ as 01 for state X, 00 for state Y, and 11 for state Z. You are to assume that you will never reach the state $S[1:0]=10$, so you don't care what happens in that case. You must show your work to get any credit! *You only need to compute the next state and output logic, you don't need to draw the gates or flip-flops!* Place your answer where shown, all answers must be in minimal sum-of-products form. [14 points]



(Be sure all are in minimal sum-of-products form!)

NS1= _____

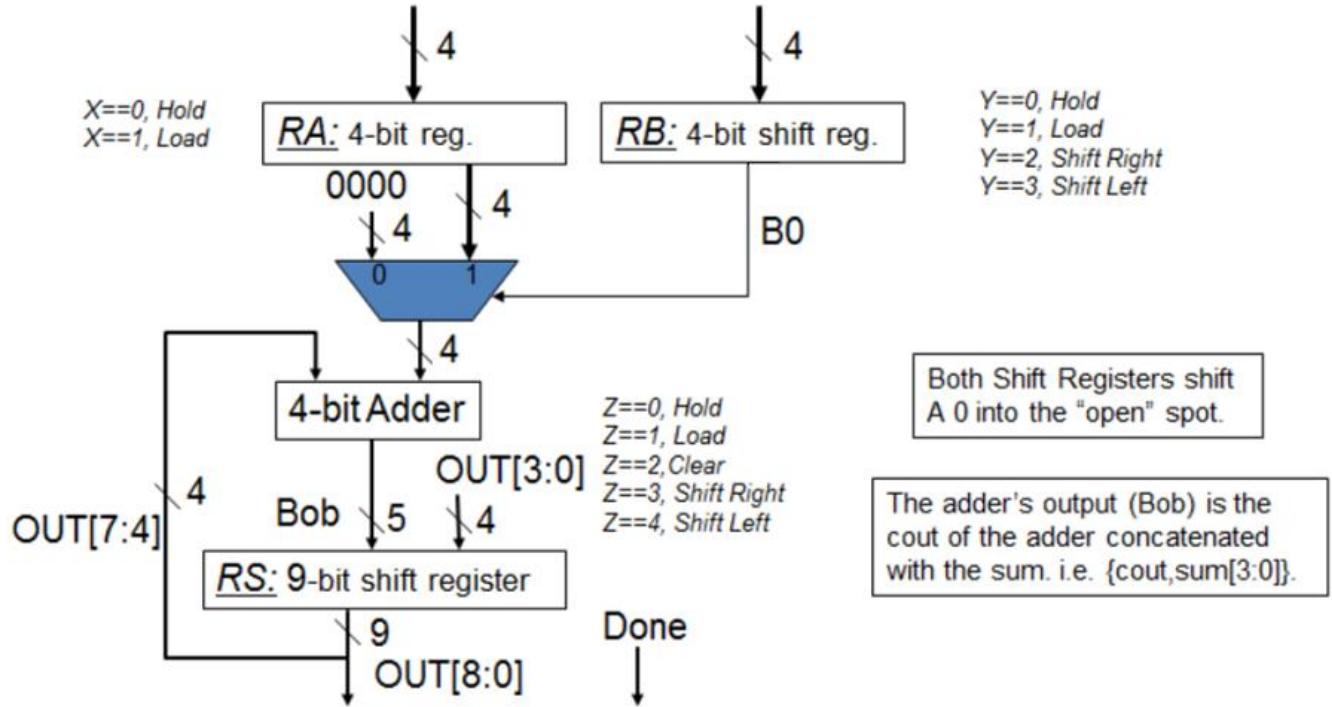
NS0= _____

W= _____

6. The following circuit is an unsigned binary multiplier which computes $A \cdot B$. Draw the control state transition diagram. [15 points]

You are to assume:

- Start will be asserted for one cycle and that A and B are available on the rising edge that start is asserted
- On any rising edge Done is asserted, Sum should be correct.
- Done need only be held high for 1 cycle.
- Start will not be reasserted to start a new operation until after you assert Done (and if it is, you can ignore it).



7. Binary Coded Decimal (BCD) encoding is used to represent decimal numbers. Each digit of the decimal number is binary encoded with 4 bits. For example, 12 will be encoded as 0001 0010 and 45 as 0100 0101.

Using gates and two 4-bit counters of the type to the right, design a two-digit *saturating* BCD counter that counts from 00 to 99. Your BCD counter should have three inputs: clock, reset and enable. On each rising edge:

- If reset is a 1, your BCD counter should go to 00.
- Otherwise, if enable=1 it should increment to the next value (staying at 99 if already at 99).
- Otherwise it should hold its value.

It should have outputs LSD[3:0] which is the least-significant BCD digit and MSD[3:0] which is the most-significant BCD digit. Your grade for this problem will be based on correctness, efficiency, and clarity. Your counters must be clocked using the “clock” input. Assume the supplied 4-bit counter will ignore the EN input if RESET is 1. **[15 points]**

