EECS 270 Final

Spring '05, Dr. Mark Brehob

Name: _____ UM ID: _____

Sign the honor code:

I have neither given nor received aid on this exam.

_____

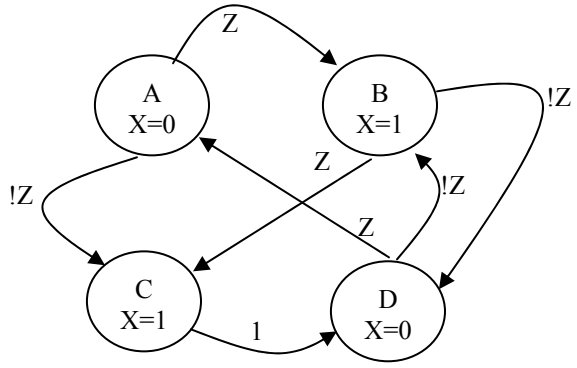
Scores:

#	Points
1	/25
2	/10
3	/10
4	/13
5	/15
6	/18
7	/9
Total	**/100**

NOTES:

- This exam will last 120 minutes.
- Throughout this exam * = AND, +=OR, !=NOT $\oplus$ = XOR
- Open book (our text only!), open notes. No computers, cell phones, or other communication devices.
- There are 10 pages including this one. The last page is solely for reference.

1. Consider the following state-transition diagram:

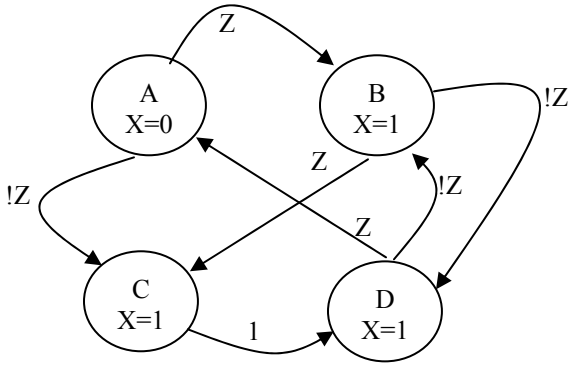


State	Q_1Q_0
A	00
B	01
C	10
D	11

For this entire problem, use the state mapping shown above.

a) Consider the FSM that implements the above state-transition diagram. Write the logic equations the next-state logic (Q_1* and Q_0*) as well as the output logic. You are to use **minimal *product-of-sums*** and must clearly show your work. **[12]**

b) Using Verilog, write the **next-state** logic block. You are to use a case statement and must define any constants and variables which you wish to use. *You may not simply use the logic equations*, you must use case statements as we have in the lab. Syntax errors that imply a lack of understanding of Verilog will result in point loss. A copy of the figure is provided below. You must use the same state mappings as before. **[13]**



2. Using static CMOS logic, implement the function !(A*C+B*C). You have both the input variables and their negations available as inputs (so **A, B, C, !A, !B, and !C**). You will lose 4 points if you use more than 8 transistors. **[10]**

3. Design a Moore-type state transition diagram for a state machine that has one input (X) and one output (A). The output should go high if the last three instances of X were the same. Otherwise the output should be low. You must use fewer than 9 states. **[10]**

4. Your boss has provided the FSM found below. She has provided the following characteristics for the logic family being used: **[13]**

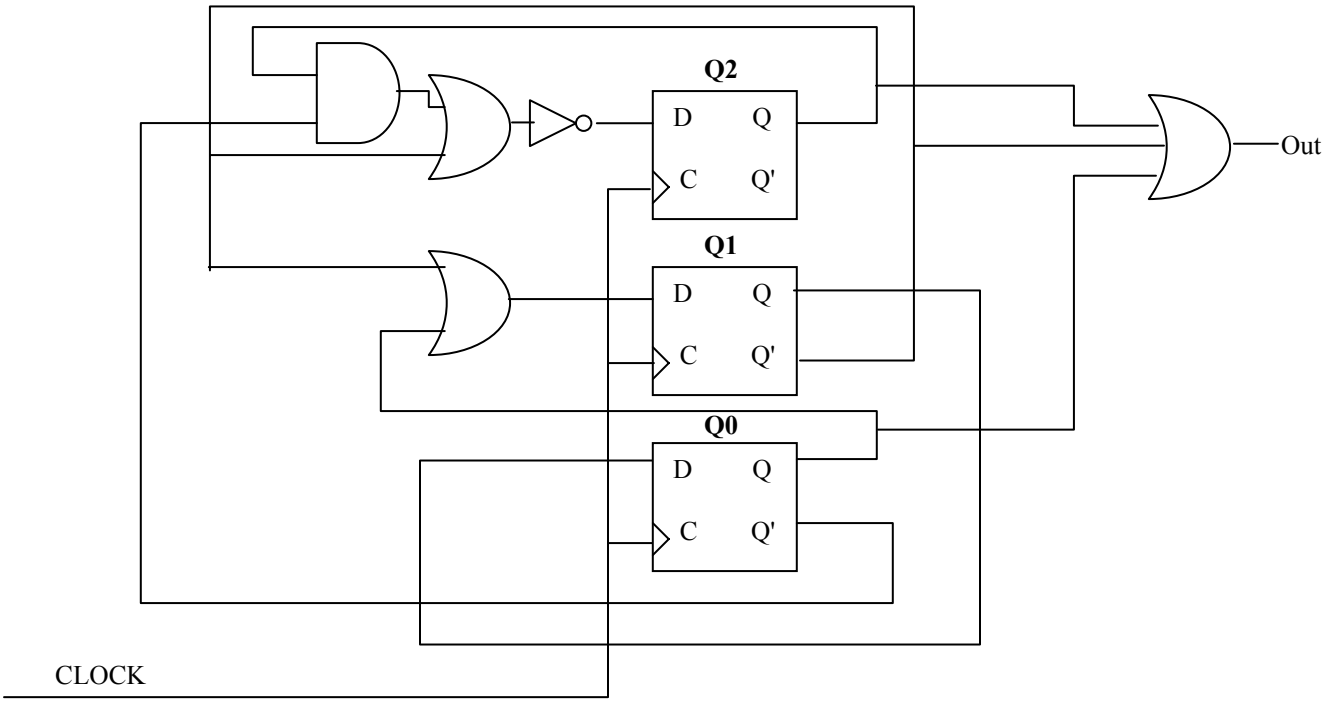
Device name	**Min Delay**	**Typical Delay**	**Max Delay**
Inverter	10ps	20ps	30ps
2-input AND gate	20ps	50ps	70ps
2-input OR gate	20ps	40ps	60ps

Device	**Clock to Q**			**Set-up time**	**Hold time**
	Min Delay	Typical Delay	Max Delay		
D-flip-flop	10ps	15ps	20ps	30ps	20ps

a) What is the fastest this FSM can be safely clocked in a consistent manor (provide your answer in decimal MHz). Show your work. **[6]**

b) As drawn the circuit would be expected to occasionally fail even with a low-frequency clock. Why? **[3]**

c) Make changes to the circuit so that it still performs the same logical function but fixes the problem identified in part "b". Your changes should not change the fastest clock frequency allowed (from part a). **[4]**



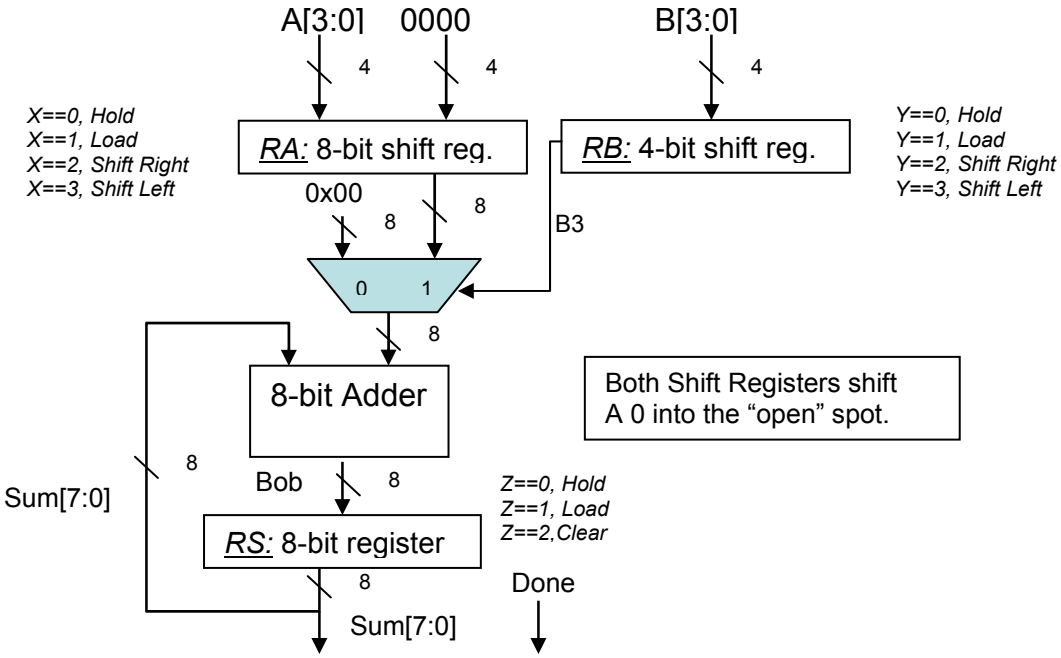
5. Consider a self-controlled car that is to be designed to follow tape found on the floor. You are to design the controller according to the following specifications.

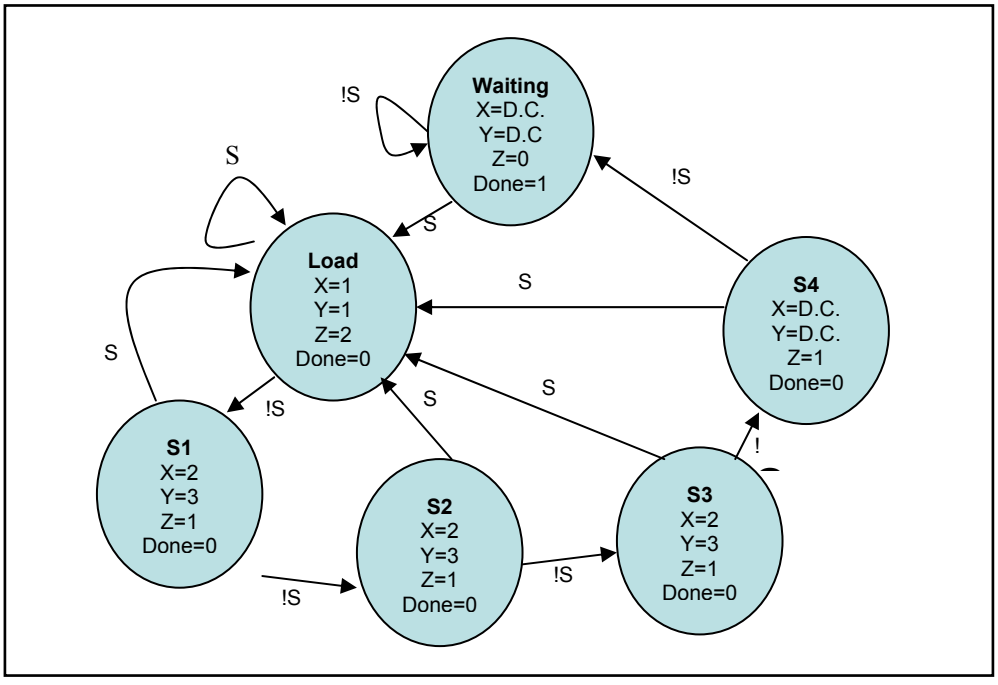
   - The controller gets data from two sensors, one on the left and one on the right side of the car. The sensors (named "L" and "R") output a "1" if the tape is below the car and a "0" otherwise.
   - The controller has one two-bit output named "S". If S[1:0]=0 the car will go straight. If S[1:0]=1, the car will go left and if S[1:0]=2 the car will go right. The value S[1:0]=3 should never be used.

   - If the left sensor detects the tape and the right sensor does not, the car should turn left.
   - If the right sensor detects the tape and the left sensor does not, the car should turn right.
   - If both sensors detect the tape, the car should go straight.
   - If neither sensor detects the tape the car should to left if it was last going left, otherwise it should go right.

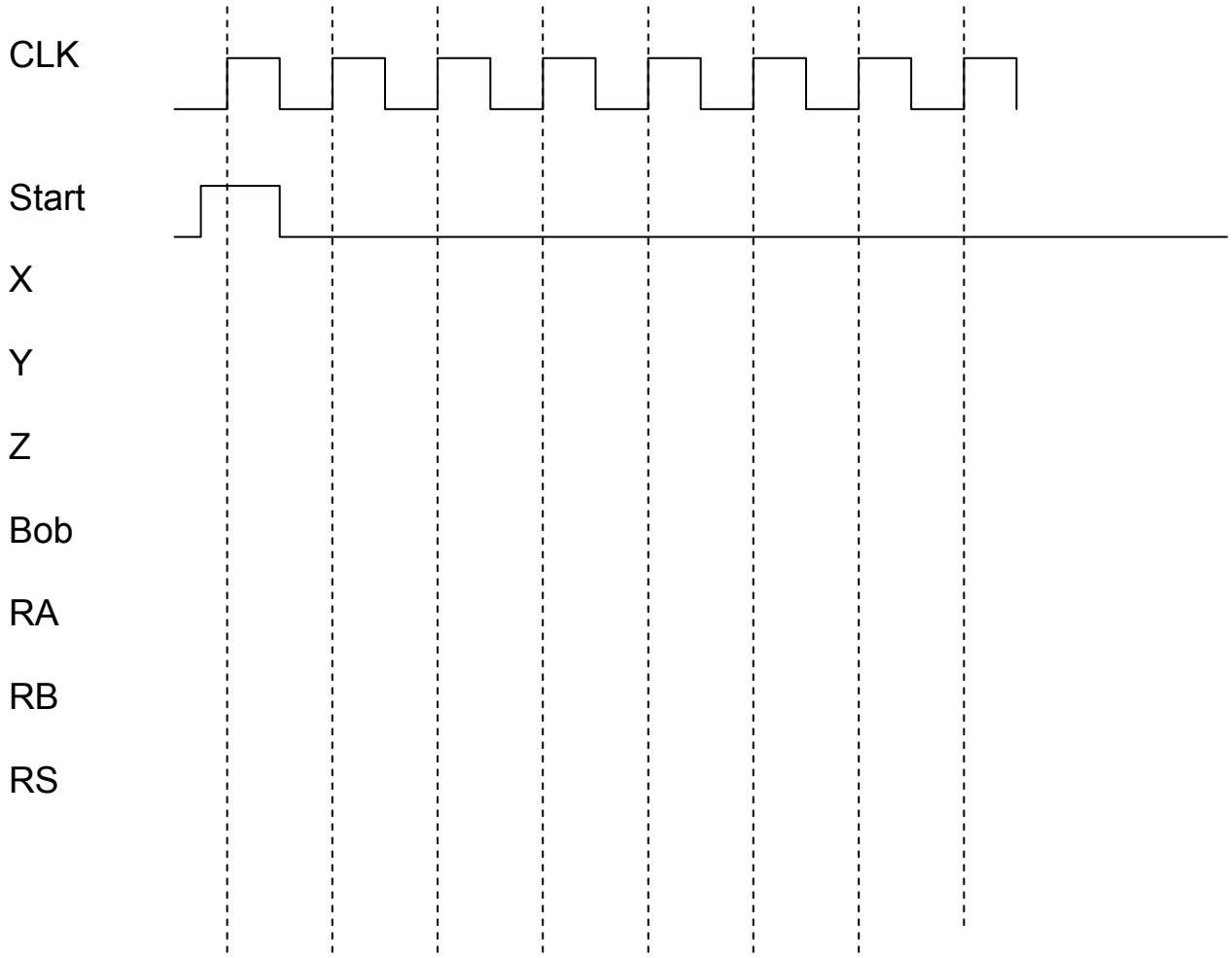
   Design a state-transition diagram that implements this controller. *It is to use as few states as possible*. **[15]**

6. On this page is a slightly modified data-path and state transition diagram for our shift-and-add multiplier. *It doesn't quite work correctly.* On the following page you will be asked some questions about it. The last page of this exam is a copy of this page that you can rip out for reference.





a) Fill in the following values. Use base-10 numbers. You are to assume that $A=1011_2$ and $B=1101_2$. Show all states up to and until "Waiting" is entered. If you can't determine a value, indicate that by writing an "X" in place of the value. **[12]**



b) Using only a few sentences, explain the simplest change(s) you can which would allow this multiplier to work correctly. This will be graded based on correctness, conciseness, simplicity and clarity of explanation. **[6]**

7. You have designed a system that transmits one of four 5-bit codes A, B, C, D, shown below, across a microwave link.

A: 0 1 1 1 0
B: 1 1 0 1 0
C: 0 1 1 0 1
D: 1 0 0 1 1

a) What is the Hamming distance of this code? Show your work. **[5]**

b) Your manager explains to the customer that the microwave link is very robust and only a single bit in any 5-bit code can be flipped. If the data transmitted by the microwave link is corrupted and you receive the code X, shown below, can the received code be corrected? If yes, what was the transmitted code? If no, what is the set of possible transmitted codes? Do the same for Y. **[4]**

X: 11000

Y: 01100

This page can be ripped out and need not be turned in! It is used for problem #6.