EECS 270 *Final Exam*

Spring 2011

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

_____

Scores:

Problem #	Points
1	/14
2	/10
3	/6
4	/16
5	/12
6	/12
7	/10
8	/10
9	/10
Total	**/100**

NOTES:

1. Open book (our text only) and Open notes
2. Calculators are allowed, but no PDAs, Portables, Cell phones, etc.
3. Don't spend too much time on any one problem.
4. You have about 120 minutes for the exam.
5. *Be sure to fully label any MSI device you use.*

Be sure to show work and explain what you've done when asked to do so

Fill-in-the-blank/multiple choice

14 points, -2 per wrong or blank answer.

1)

a) A 10-bit 2's complement number can represent values from _____ to _____. (Your answers are to be in decimal)

b) If you treat 100010 as a 6-bit unsigned number its decimal value is _____. If you treat it as a 6-bit 2's complement number its decimal value is _____.

c) A *sum* term in which each of the variables appears once is also called a ***minterm / maxterm / hyperterm / minimal terms***.

d) The *minimal* sum-of-products representation of (A'+B')*(A'+B) is _____.

The *cononical* sum-of-products representation of that equation is _____.

e) Say a given D flip-flop is clocked at 100MHz, has a 2ns set-up time, 3ns hold time and 4ns clock-to-Q delay. Approximately ***1 / 10 / 20 / 50 / 80 / 90 / 99*** percent of the time changes to the flip-flop's D input aren't allowed.

f) For the following Verilog code, what should the variable declarations be?

```
assign a = b & c;
always@*
begin
   b = a;
   c = b;
end
```

```
a) reg a, b, c;
b) wire a, b, c;
c) wire a, b;
   reg c;
d) wire a;
   reg b, c;
e) any of the above
```

2) Using the provided tables, find a minimal sum-of-products solution and a minimal product-of-sums solution for the equation $F=\sum_{A,B,C,D}=(0,4,5,6,7,10,13,15)+d(1,12)$. Clearly show your work. **[10 points]**

AB/CD	00	01	11	10
00	1	1	d	0
01	d	1	1	0
11	0	1	1	0
10	0	1	0	1

AB/CD	00	01	11	10
00	1	1	d	0
01	d	1	1	0
11	0	1	1	0
10	0	1	0	1

Minimal sum-of-products: _____

Minimal product-of-sums: _____

3) Find the minimal sum-of-products for the following equation. You may use any method. **[6 points]**

$$F=\sum_{A,B,C,D,E}=(0,8,16,31)+d(15,25)$$

4) Provide a state diagram for the following problem. There is one input (A) and one output (Z). If A has been a 1 for two successive cycles *at any point since reset* the output should be 1. In addition, if A has been a zero for the *last two cycles* the output should also be 1. Otherwise the output should be 0.

Example:
A:0100100010110001
Z:0001001100011111

a) Design a state diagram with Moore-type outputs that implements this. For full credit, you should use no more than 5 states. **[8 points]**

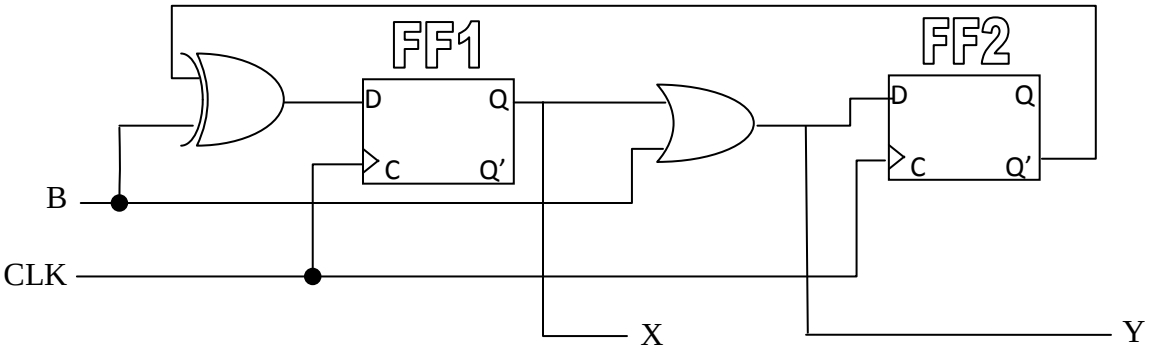
b) Design a state diagram with Mealy-type outputs that implements this. For full credit, you should use as few states as possible. **[8 points]**

5) Reduce the number of states in the state table as much as possible using the partitioning method as done in class and the text. The initial state is F. Clearly show your work and draw the reduced-state diagram. **[10 points]**

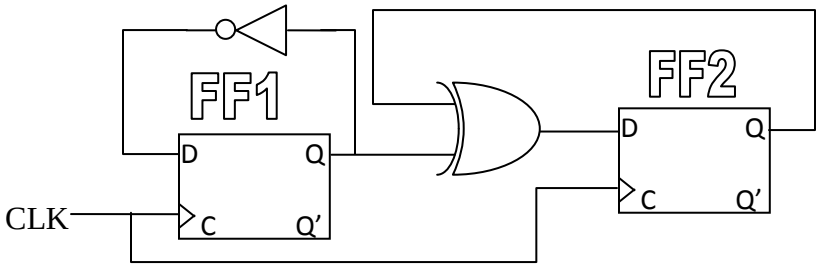
Present state	Next State **x=0**	**x=1**	Output **z**
A	A	B	0
B	B	E	1
C	A	E	1
D	D	C	1
E	A	C	1
F	A	C	0

A					
B					
C					
D					
E					
	F	**A**	**B**	**C**	**D**

6) Draw the state-transition diagram associated with the circuit below. **[12 points]**



7) Consider flip-flops FF1 and FF2, each nominally clocked off of the same clock. Assume:
   - Each flip-flop has a set-up time of 5ns
   - Each flip-flop has a clock-to-Q delay of 2ns to 4ns.
     - The clock to Q delay is the same to Q and Q'.
   - The XOR gate has a delay of 2 to 6ns.
   - The NOT gate has a delay of 1 to 4 ns.
   - Flip-flop FF1's rising edge may be as much as 2.5 ns before FF2's rising edge or as much 1.5ns after.



a) What is the fastest clock period you could safely clock this system at? **[5]**

b) What is the (non-negative) range of values for the hold time that would be sufficient? **[5]**

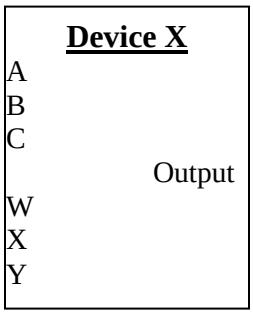
8) You are to implement "Device X". It takes six inputs and generates a single bit of output as described by the truth table below. (Note that "x" indicates don't care, so for example if ABC=011 and WXY=010, the output should be 1).

Design a circuit that implements this device using no more than three of the following devices (you may use a device more than once if you wish but each time counts as a use):

- 2 to 4 decoder, 4 to 1 MUX, 4 to 2 MUX, 4 to 2 encoder, 4 to 2 priority encoder, 4-input AND gate, 4-input OR gate, 4-input NOR gate, and 4-input XOR gate.

You will be graded on functionality and clarity of your answer (in other words, be very careful to properly label each device you are using and make it clear what each inputs and outputs is connected to). You may freely use ground and power as needed. **[10 points]**

A	B	C	Output
1	x	x	W
0	1	x	X
0	0	x	Y



9) Using standard NMOS and PMOS transistors, implement a circuit which creates an output that matches the following truth table using 8 or fewer transistors. A, B and C are inputs, OUT is the output. You only have the non-inverted values of A, B and C. **[10 points]**

A	**B**	**C**	**Out**
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	HiZ
1	1	1	0