EECS 270 *Final Exam*

Spring 2022

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

_____

NOTES:

1. ***The exam is open book and open notes. You may not use any device capable of communication (cell phones, calculators with wireless, etc.)***
2. You have about 120 minutes for the exam total.
3. Some questions may be harder than others. Manage your time wisely.

4. If you need additional room for an answer, the last 2 pages are blank and you may use them as part of your answer. Just be sure to indicate you've done so on the page of the question.

1. Fill in each blank or circle the best answer. **[15 points, -2 per wrong or blank answer, min 0]**

   a) !A!C+BC has _____ as a prime implicant
   - !AB!C
   - !A!BC
   - !AB
   - AB

   b) The 6-bit 2's complement representation of -7 is _____.

   c) If a given function has A, B, C, and D as inputs, there are _____ minterms in the equation A+B.

   d) A 4-bit 8-to-1 mux requires _____ select inputs.

   e) You are building a memory where each address references 8 bits of data. You are using a 1024 by 1024 memory array to do so. The row decoder needs _____ bits of address while the column mux requires _____ bits of address.

   f) Write 13.1_8 as a binary number: _____

   g) A 3-input XNOR gate has _____ minterms.

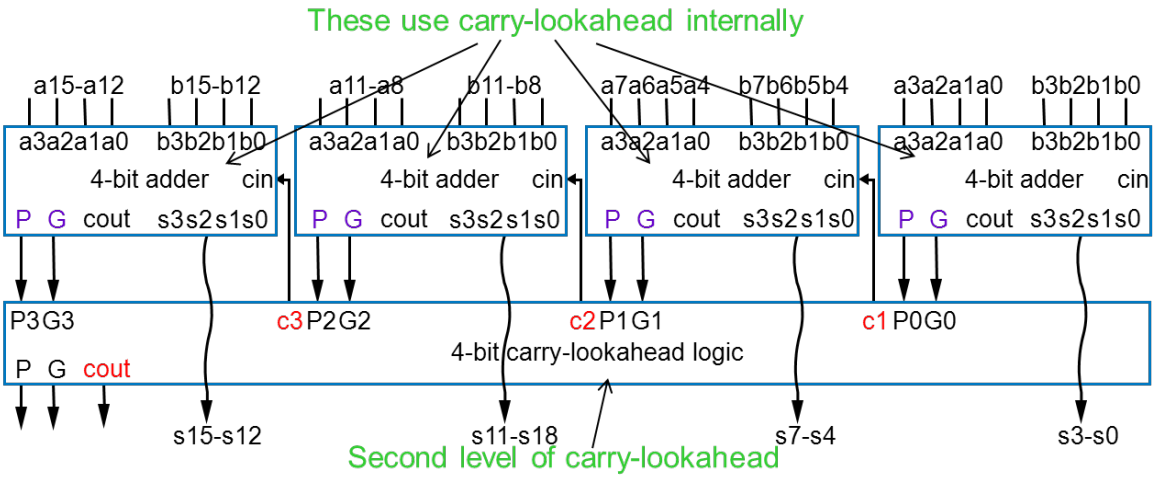
   h) A 3-input NOR gate can be implemented with as few as _____ transistors in static CMOS.

   i) _____ is/are form(s) of volatile memory.
   - DRAM
   - SRAM
   - Neither DRAM nor SRAM
   - Both DRAM and SRAM

2. Say we are using the 16-bit carry-lookahead adder taught in class (and seen below) to add 0xf1f0 to 0x0fff. Provide binary values for each of the following: **[8 points, -2 per wrong bit, min 0]**

   a) P[3:0] = _____

   b) G[3:0] = _____



Note: P[3:0] and G[3:0] refer to the values labeled P3, P2, etc. in the "second-level of carry lookahead logic".

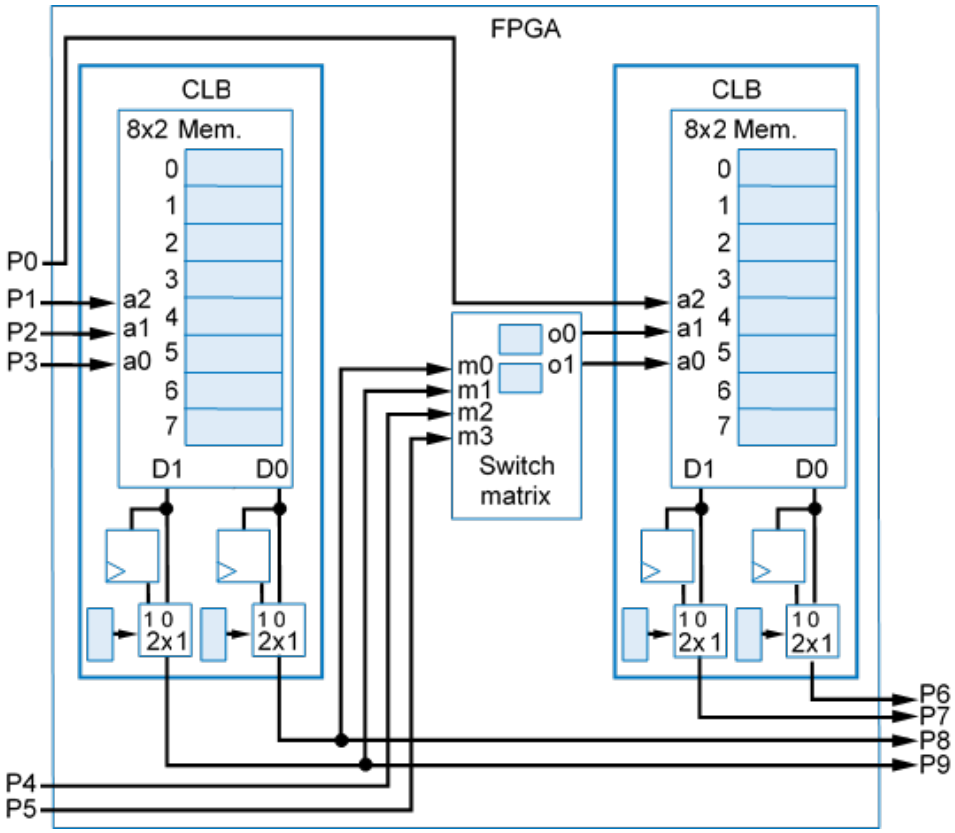
3. Implementation **[12 points]**

   a) Design a 3-input AND gate in static CMOS using 8 or fewer transistors. **[6]**

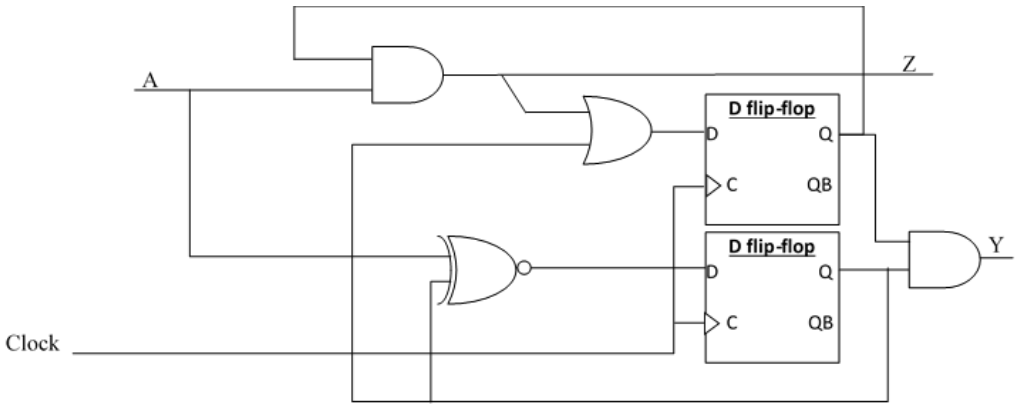
   b) Implement the circuit AB+!BC using only 2-input NAND gates. You have only A, B, and C (not their inverses) available as input. For full credit you must use as few NAND gates as possible. **[6]**

4. Using a Kmap, find the minimal *product-of-sums* for $A=\Sigma_{(W,X,Y,Z)}=(1, 3, 7, 8, 9, 10) + d(4, 5)$. Clearly show your work. **[6 points]**

P0	P1	P2	P3	P4	P5	P6	P7	P8	P9
			A	A		Y	Z		



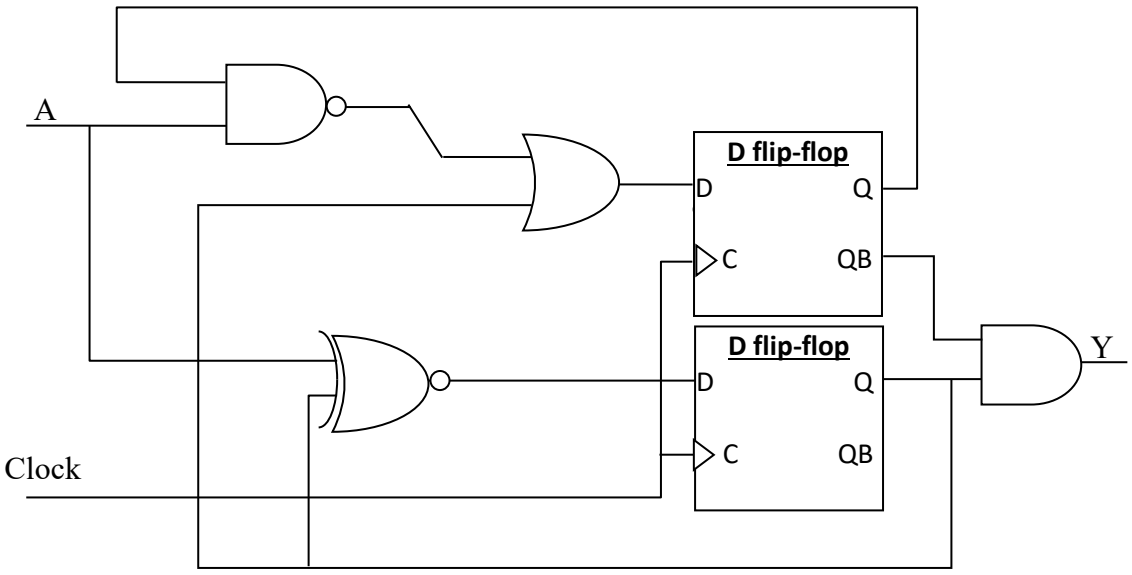
5. Fill in blank boxes as needed to implement the following circuit. Leave boxes blank if their values don't matter. You may use temporary values to connect outputs back into inputs. Be sure to use the names given (A, Z, etc.) **[12 points]**



	Min	Max
OR/AND	3ns	5ns
NOR/NAND	2ns	3ns
NOT	1ns	2ns
XOR/XNOR	2ns	6ns

DFF:		**Min**	**Max**
	Clock to Q	2ns	3ns
	Set-up time	4 ns	
	Hold time	6 ns	

6. Assuming the input A ***always*** arrives 2ns after the rising edge of the clock, answer the following questions. **[12 points]**
   a) Where do inverter pairs need to be added needed to ensure that there are no hold time violations? Add them in a way that maximized the frequency this circuit can be clocked at. *If there is more than one way to add inverter pairs which maximizes the frequency of the circuit, add as few as possible.* You may not make any changes other than adding inverter pair(s). **[6]**
   b) What is the lowest clock period that could be safely used to clock this circuit (after taking into account the changes you made above)? Clearly show your work. **[6]**

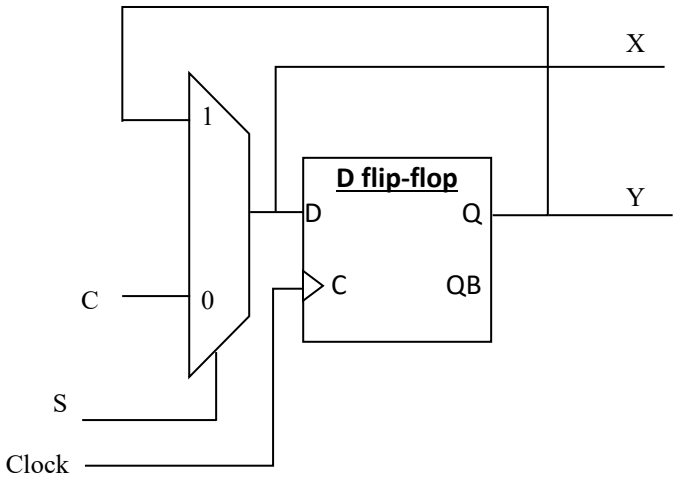


7. Design a Mealy-type state-transition diagram which has two inputs, A and B, as well as one output, S. A and B are to be treated as binary values where the least-significant bits are provided first and S is to be the sum of those two numbers so far (again least significant-bits first). For example, the given inputs A and B would create the output S as shown. **[12 points]**

```
A=110100
B=011100
S=100110
```

The above example has A as 001011 (reversing the order) which is 11_{10} and B as 001110 which is 14_{10}. The sum, S, is 011001, which is 25_{10}.

8. Write a Verilog module, Bob, which implements the following circuit. The inputs are S, C, and Clock. The outputs are X and Y. The code must be correct, clear, and reasonably concise to get full points. **[10 points]**

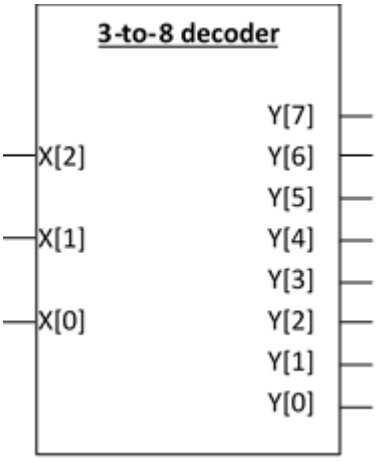


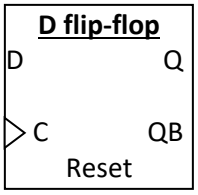
9. Consider a state machine with the following truth table where S1 and S0 are the current state, A is an input, N1 and N0 are the next state (for S1 and S0 respectively) and Z is an output. **[13 points]**

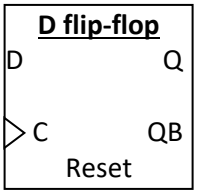
S1	S0	A	N1	N0	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	1	1
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1

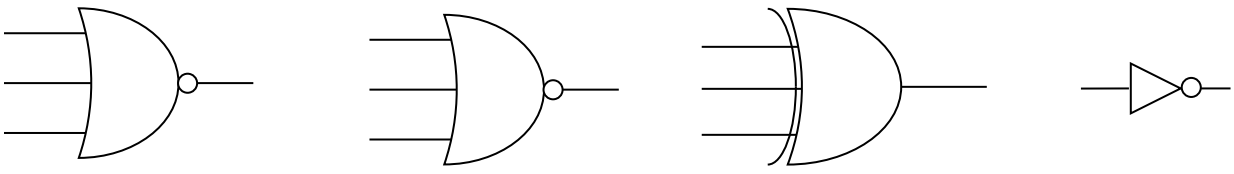
   a) Circle the best answer for the following **[2]**
   - Z best characterized as a ***Mealy / Moore*** output.
   - If S[1:0]=00 is the initial state, all states ***are / are not*** reachable.

   b) You have two D flip-flops, a 3-to-8 decoder, two 3-input NORs gate, a 3-input XOR gate and an inverter. Design a circuit which implements this state machine. **Clearly label inputs and outputs.** You may draw lines or connect things by name as you wish. **[11]**









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