EECS 270 *Practice* Midterm

Spring '04, Prof. Mark Brehob

Name: _____ UM ID: _____

Sign the honor code:

I have neither given nor received aid on this exam.

_____

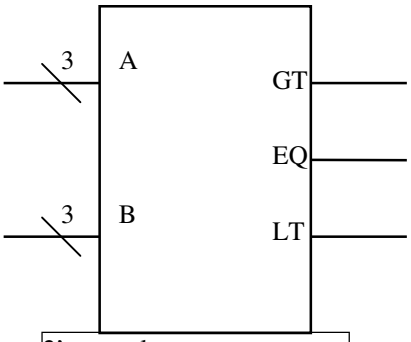
Scores:

#	Points
1	/20
2	/15
3	/12
4	/10
5	/20
6	/8
7	/15
Total	**/100**

NOTES:

- This exam is intended to be taken in 120 minutes.
- Throughout this exam * = AND, += OR, != NOT
- Some other things to be ready for on the actual exam: signed-magnitude and excess notation, tri-state buffers, carry look-ahead adders, subtraction, error correction/hamming distances and multiplication. Of course there may be other things too…
- Open book, open note.

1. Your boss has asked you to design a comparator for three-bit 2's complement numbers. **[20]**



2's complement comparator

A[0:2] and *B[0:2]* are both 2's complement numbers with *A2* and *B2* being the MSBs. If A>B then *GT* should be 1 and the other outputs 0. If A<B then *LT* should be 1 and every other output 0. If A=B then *EQ* should be 1 and every other output 0.

(recall that MSB= Most Significant Bit)

a) List the following 3-bit 2's complement numbers in order from smallest to largest: 111, 101, 011, 010, 100. **[4]**

b) Write the logic equations for GT, EQ and LT. Be sure to circle your final answer. Be sure you have also circled any intermediate values (nodes) you are using in your final answer. **[16]**

2. Find the minimal sum-of-products of the following logic **equation using the Quine-McCluskey algorithm**. You must ***clearly*** show your work for credit. Solving the problem in some other way will result in 0 points. **[15]**
$\Sigma_{A,B,C}(0,1,2,4,5)$

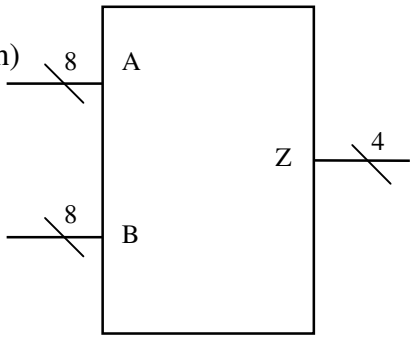
3. Using the rules of logic convert the following into sum-of-products form. You must show each step and state which rule you are using at each step. **[12]**

   !(A*B)*(C*D)

4. Find the ***minimal <u>product-of-sums</u>*** for the following equation. You may use any technique. **[10]**
   !(A+B+C) + (B*!C) +(A*!B)

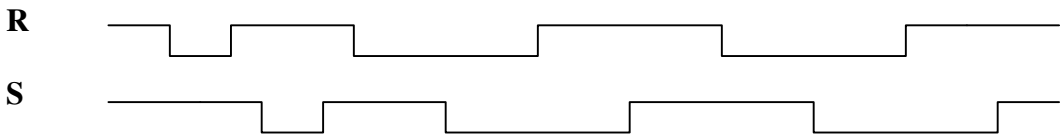
5. Consider a very unusual adder. It takes two 8-bit inputs, both representing number using the "one hot" representation scheme (Thus the inputs range in value from 0-7). The output is a 4-bit unsigned number that is a sum of the two inputs. In your design you may use the following devices: (Be sure to ***label*** all of the devices you use other than standard gates!) **[20]**
    - 2-input AND gates, 2-input OR gates, 2-input XOR gates, NOT gates
    - 3-bit adders (inputs and outputs are both 3-bits) with carry-in and carry-out.
    - 8 to 3 encoders (all wires active high)
    - 3 to 8 decoders (all wires active high)
    - 8 to 4 Multiplexers (all wires active high)

The inputs A[7:0] and B[7:0] are describing input values ranging from 0 to 7 using the "one hot" representation scheme. The output Z[3:0] is to be the sum of the values of the 2 inputs. Z is represented as an unsigned number. For the inputs A7 and B7 are the MSBs. While for the output Z3 is the MSB.



Unusual "one hot" adder

6. Show the values one would expect for Q and QN given the following inputs on an S-R latch. **[8]**



Q

QN

7. Consider the state-transition diagram shown below.
   a) If we were to start in state 00 and the input pattern were 001001, what state would we be in? **[3]**

   b) Design a state machine that implements this state transition diagram. **[12]**