Quiz 1 – Spring 2022 – EECS 270

Name: Key uname: key

This quiz is graded out of 100 points. Please remember you can drop your lowest quiz score. You will have 20 minutes for the quiz. It is closed book and closed notes. Show your work.

1. Write the **canonical sum-of-products** for the following truth table. **[25 points]**

X	Y	Z	A
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

A= $\bar{X}\cdot\bar{Y}\cdot Z + \bar{X}YZ + X\bar{Y}Z$

000 111
111 cc 6

2. Fill-in-the-blank **[25 points, -5 for each wrong or blank answer]**

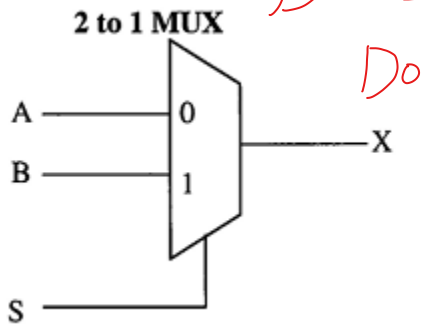
   a. The 6-bit 2's complement number representation of -7 is 111001.
   -32 16 8 1 c

   b. The range of representation for a 4-bit signed-magnitude number is from −7 to 7.

   c. According to the Commutative theorem of Boolean algebra, A+B = B+A.

   d. (A+B)*(A+C) = A + B·C according to the distributive theorem.

3. Implement a 1-bit 2-to-1 MUX using only NAND gates. For full credit, use 4 or fewer NAND gates. The inputs and outputs should be as labeled in the figure below. **[25]**



4. Using only the devices listed below, design a circuit which takes two 3-bit unsigned numbers (A[2:0], B[2:0]) as input and outputs a 4-bit unsigned number (X[3:0]). If A=B, the output should be "0", otherwise the output it should be A+1.

   Example: if A[2:0]=2 (010) and B[2:0]=4 (100) the output should be X[3:0]=3 (0011)

   In your design you may use the following devices (as well as freely using "0" and "1" as a inputs as desired)

   - AND, OR, and XOR gates (any number of inputs)
   - Inverters
   - 1-bit 2 to 1 MUX
   - 3-bit unsigned adder (Inputs: A[2:0], B[2:0]; Outputs: S[2:0], Cout)
   - 4-bit 2 to 1 MUX
   - 8 to 3 priority encoder (Inputs A[7:0]; Output: X[2:0]).

   You must clearly label any device you use (other than gates and inverters) and your design should be clear enough that someone else could understand how everything was to be connected. Your grade will be based in part upon the efficiency and clarity of your design. **[25]**