

Quiz 2 – Spring 2022 – EECS 270

Name: _____ uname: _____

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! To receive partial credit, work must be shown.

1. Write the **canonical product-of-sums** for the following truth table. [20 points]

| X | Y | Z | A |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

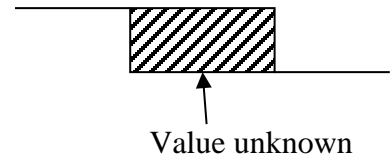
A= $(X+!Y+Z)*(!X+Y+Z)*(!X+!Y+!Z)$

Notice this is Product-of-Sums!

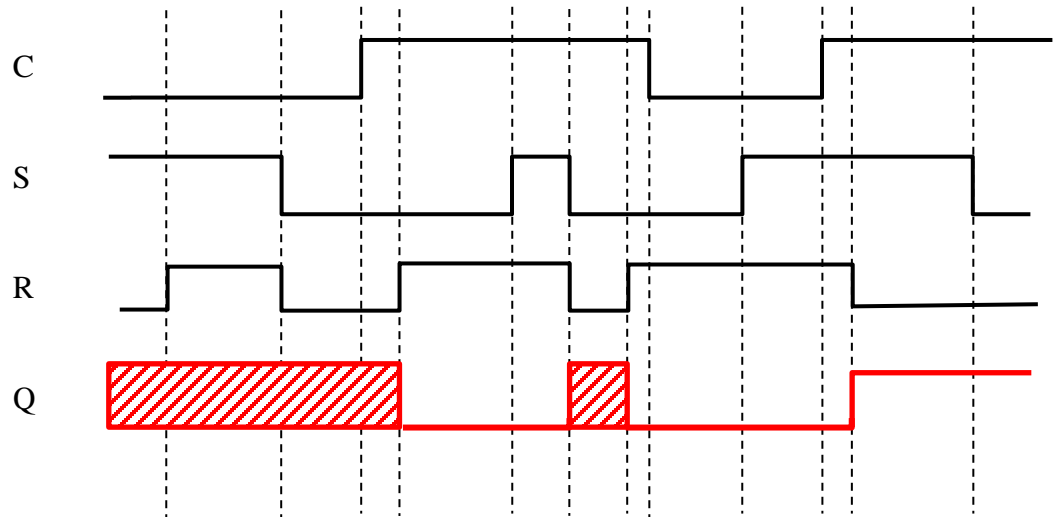
2. Fill-in-the-blank [20 points, -5 for each wrong or blank answer]

- a. The time *before* the rising edge of the clock when no input should be changing is called the setup time
- b. 11110111 is -9 as an 8-bit 2's complement number
- c. A signal with a frequency of 100MHz has a period of 10 ns
- d. $(A*B)+(A*C) =$ $A*(B+C)$ according to the distributive theorem.

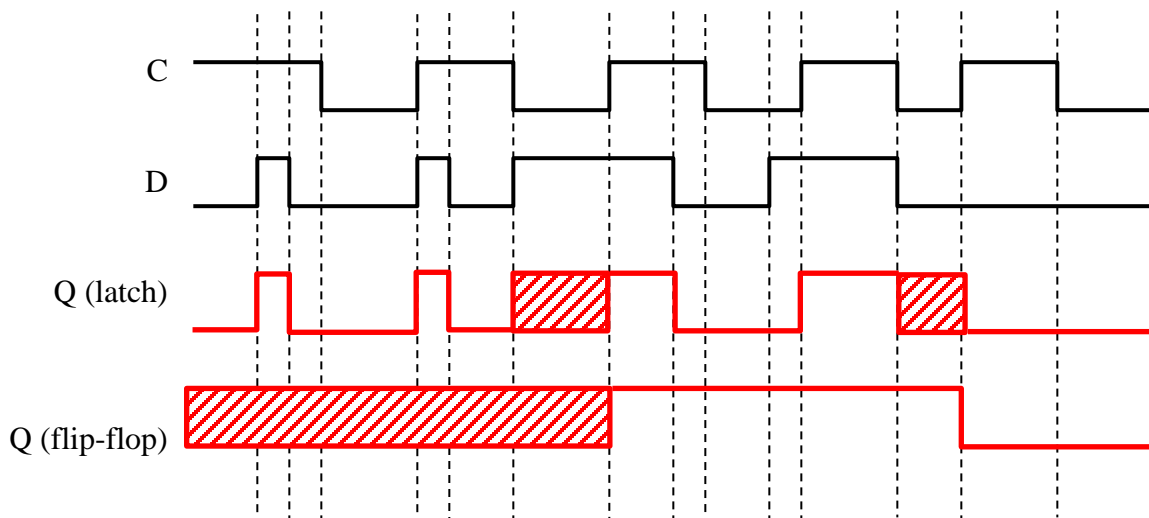
3. Complete the following timing diagrams. If the value is unknown (or oscillating) at some point, clearly indicate that with hashes (as shown).



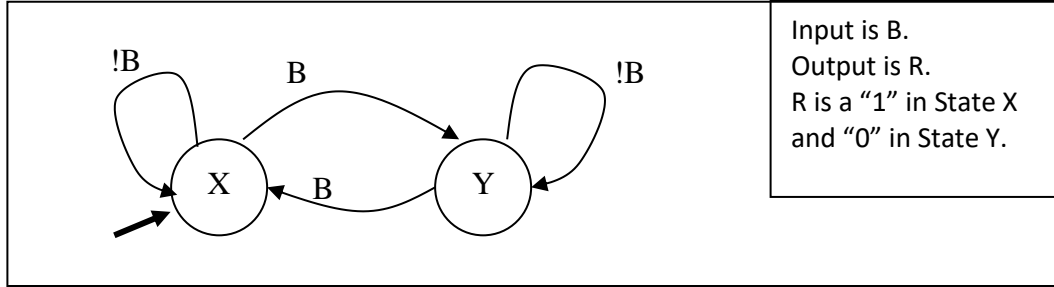
- a) Complete the timing diagram below for an SR latch with enable. [10 points]



- b) Complete the timing diagram below for both a D latch and a D flip-flop. [20 points]



4.



Draw flip-flops and gates which implement the above state transition diagram. All flip-flops are set to 0 when the system is initialized (to the initial state should be where the flip-flop(s) are zero).

Your answer will be graded in part on clarity and simplicity. **[30 points]**

X needs to be the 0 (reset) state so Y is 1.

| S | B | NS |
|---|---|----|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

