Quiz 2 – Spring 2012 – EECS 270

Name: _____ uname: _____

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! To receive partial credit, work must be shown.

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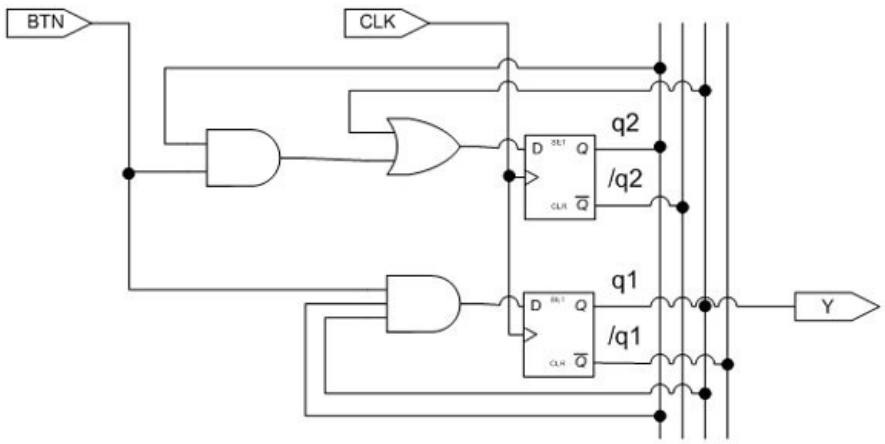
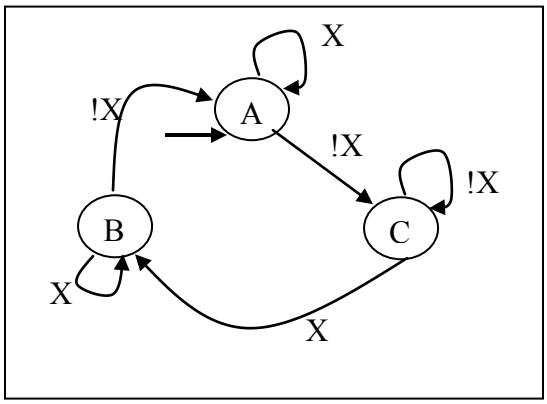
1. Say you have one input, X as well as a single output Y. Provide a state-transition diagram where Y goes high iff the last three values of X were "001" **[30]**

Device	Min	Max
DFF:		
Clock to Q	1ns	4ns
Set-up time	3ns	
Hold time	1ns	
OR/AND	1ns	4ns



2. Given the circuit and timing information above, what is the lowest clock period you can clock this circuit at? (Hint: the hold time is met so you don't need to add any inverter pairs.) You should assume that the inputs are coming from flip-flops and the outputs are going to flip-flops. *Clearly show your work.* **[25]**

3. Consider the following state-transition diagram:



There is one output, Z, which is 1 when in state A or B and 0 in state C.

Using only AND, OR, and NOT gates (including freely using bubbles) as well as D flip-flops, *neatly draw* the state machine for the above state-transition diagram. You are to use an encoding of A=00, B=11, and C=01 for the states. Finally, any unused state encodings should be treated as don't cares. You'll need to show your work to get much in the way of partial credit. **[45]**