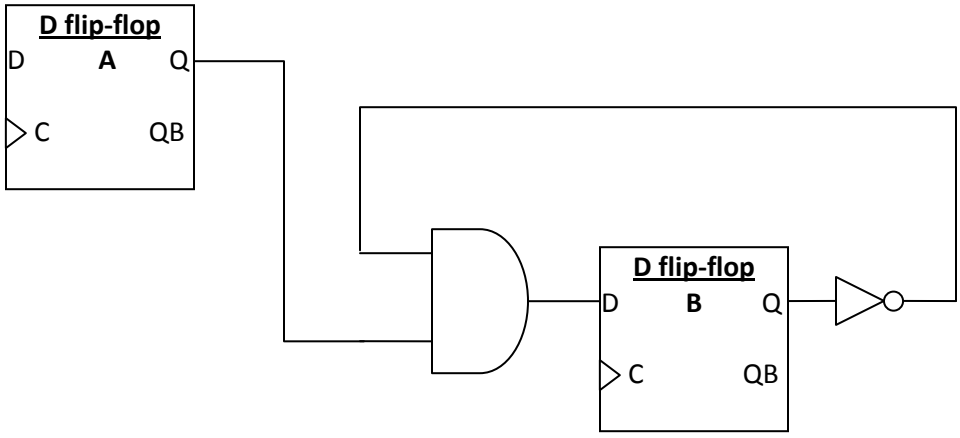
Quiz 5 EECS 270 Spring 2012. Honor code applies. 25 minutes.

Name: _____ uname: _____



1) Consider flip-flops A and B each nominally clocked off of the same clock. Briefly show your work. Assume:
   - Each flip-flop has a set-up time of 5ns and a clock-to-Q delay of 2ns to 4ns.
   - The AND gate has a delay of 3 to 8 ns.
   - The NOT gate has a delay of 2 to 4 ns.
   - Flip-flop A's rising edge may be as much as 1.25 ns before B's rising edge or as much 1.5 ns after.

   a) What is the fastest clock period you could safely clock this system at? **[10]**

   b) What is the (non-negative) range of values for the hold time that would be sufficient? **[10]**

   c) Redo part a) assuming the NOT gate always had a delay of exactly 1ns **[10]**

   d) Redo part b) assuming the AND gate always had a delay of exactly 1ns. **[10]**

2) Find the minimal sum-of-products of F using the Quine-McClusky algorithm. For this problem we'll be grading your answer primarily based on your work so be sure to be careful, clear and neat. Use the format provided. **[60]**

$F=\Sigma_{A,B,C,D}(3,5,8,10,12,13,14)$

Column I	✓
0011	
1000	
0101	
1010	
1100	
1101	
1110	

Column II	✓

Column III	✓

List of Prime Implicants (Provide in the form AB, AC', D)

_____

List of distinguished ones (provide the binary value of each distinguished one):

_____

Minimal sum-of-products: _____