

## Quiz 4 EECS 270 Spring 2013.

Name: KEY \_\_\_\_\_ username MLWB \_\_\_\_\_

Honor code:

I have not given or received aid on this quiz, nor have I observed anyone else doing so:

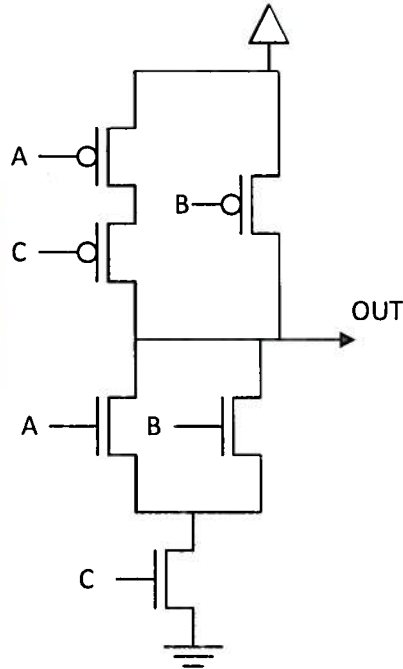
Sign here: \_\_\_\_\_

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 25 minutes for this quiz. **Closed everything including calculators!** To receive partial credit, work must be shown.

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1. Transistor to truth table [30 points, -5 per wrong or blank entry, minimum 0]

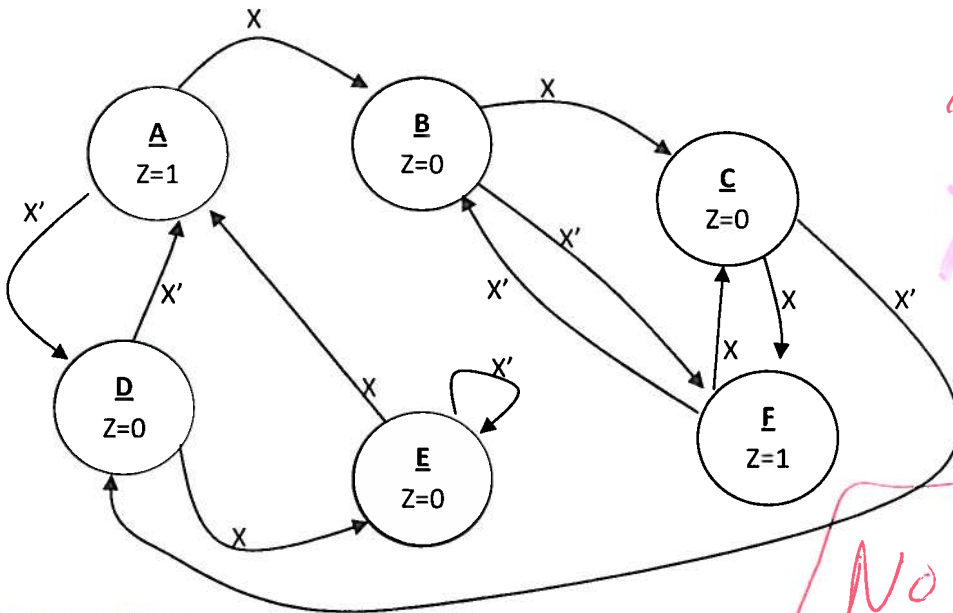
A	B	C	OUT	PUN	PDN
0	0	0	1	1	
0	0	1	1	1	
0	1	0	1	1	
0	1	1	0		0
1	0	0	1	1	
1	0	1	Smoke	1	0
1	1	0	Hi-Z		
1	1	1	0		0



Fill in the above truth table with either "1", "0", "Hi-Z" or "Smoke" (the last if OUT is connected to both Vcc and Ground).

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2. Reduce the number of states in the state transition diagram as much as possible using the partitioning method. Show your work and draw the reduced state diagram. [50]



*X = different outputs.*  
*elim. in later step.*

*No change*

A	<del>0 D B</del> 1 B C				
B	<del>0 F B</del> 1 C C	<del>F D</del> C B			
C	<del>0 D B</del> 1 F C	<del>D D</del> F B	<del>D F</del> F C		
D	<del>0 A B</del> 1 E C	<del>A D</del> E B	<del>A F</del> E C	<del>A D</del> E F	
E	<del>0 E B</del> 1 A C	<del>E D</del> A B	<del>E F</del> A C	<del>E D</del> A F	<del>E A</del> A E
	<b>F</b>	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>

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3. Using only nMOS and pMOS transistors, implement the following logic function:  $\overline{\overline{A} \cdot \overline{B} \cdot \overline{C}}$ . You will lose 10 points if your design uses more than 10 transistors. You only have A, B and C as inputs, not their inverses. [20]

$$\overline{\overline{A} \cdot \overline{B} \cdot \overline{C}} = A + B + C \Rightarrow \overline{\overline{A + B + C}}$$

