

## Quiz 4 EECS 270 Spring 2022.

Name: \_\_\_\_\_ uname: \_\_\_\_\_

**Honor code:**

I have not given or received aid on this quiz, nor have I observed anyone else doing so:

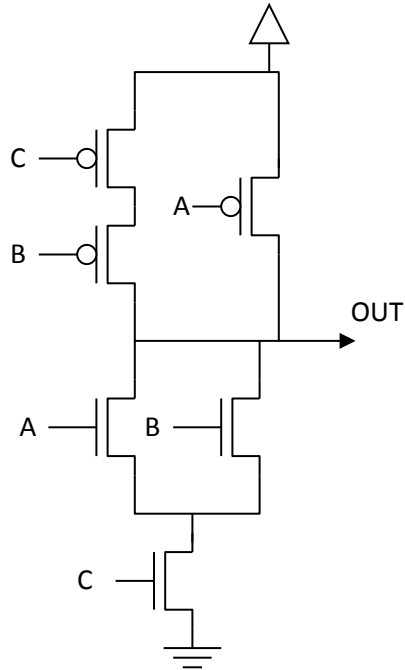
Sign here: \_\_\_\_\_

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. ***Closed everything including calculators!*** To receive partial credit, work must be shown.

---

1. Transistor to truth table [35 points, -6 per wrong or blank entry, minimum 0]

| A | B | C | OUT |
|---|---|---|-----|
| 0 | 0 | 0 |     |
| 0 | 0 | 1 |     |
| 0 | 1 | 0 |     |
| 0 | 1 | 1 |     |
| 1 | 0 | 0 |     |
| 1 | 0 | 1 |     |
| 1 | 1 | 0 |     |
| 1 | 1 | 1 |     |



Fill in the above truth table with either "1", "0", "Hi-Z" or "Smoke" (the last if OUT is connected to both Vcc and Ground).

## Quiz 4 EECS 270 Spring 2022.

2. Using a single D-flip-flop and no more than three standard gates, design a T-flip-flop. Recall a T flip-flop has two inputs: clock and EN as well as two outputs: Q and  $Q_{\text{bar}}$ . **[35 points]**

3. Say we wish to design a memory with that where each location has 8 bits of data using the figure to the right.

**[30 points]**

- a. How many addresses would you have? \_\_\_\_\_
  
- b. There are 5 blanks in the figure. Fill them each in with values that would complete our design. Let address bits be a bus named "A" and the output be a bus named D.

