

The University of Michigan
Department of Electrical Engineering and Computer Science

EECS 270 Fall 2002

Exam #1

Name: _____ UM ID: _____

For all questions, show all work that lead to your answer.

Problem #	Possible Points	Points Earned
1	16	
2	16	
3	12	
4	20	
5	21	
6	15	
Total	100	

*I have neither given nor received any
unauthorized aid on this exam.*

Signed: _____

1. (16 Points Total) Reduce the following expressions using any of the theorems or axioms of switching algebra. Note which theorems/axioms you are using.

(a: 8 pts) $A \cdot C \cdot E + A \cdot C \cdot D' + A \cdot C \cdot E' + A \cdot B \cdot D' \cdot E + B \cdot C' \cdot E$

(b: 8 pts) $A \cdot B \cdot C \cdot D + A' \cdot E \cdot F + B' \cdot E \cdot F + C \cdot D \cdot E \cdot F$

2. (16 Points Total) Perform the following number problems:

(a: 2 pts) $547_8 = ?_{16}$

(b: 4 pts) 11001_2 (two's complement representation) = $?_{10}$

(c: 4 pts) 10000_2 (one's complement representation) = $?_{10}$

(e: 3 pts) $113.33_{10} = ?_2$ (answer should be accurate to at least 6 binary places; mark any repeating digits)

(f: 3 pts) In general, what is the minimum number of bits required to approximate a decimal number in binary with an error less than 0.01 ($= 1/100$)

3. (12 Points Total) Perform the following two's complement arithmetic operations in the way a computer would perform them. Indicate if an overflow occurred *and why*:

(a: 6 pts) (5) add (-18)

(b: 6 pts) (-13) sub (+22)

4. (20 Points Total) Given the following function:

$$F = \sum_{w,x,y,z}(0, 4, 6, 7, 8, 9, 10, 11, 12, 13, 15)$$

- (a: 4 pts) Construct a K-map and circle all prime implicants.
(b: 3 pts) Mark all essential prime implicants in your K-Map.

- (c: 3 pts) Remove all essential prime implicants and mark which of the remaining prime implicants can be removed using eclipsing.
(d: 4 pts) Construct the minimal S.O.P

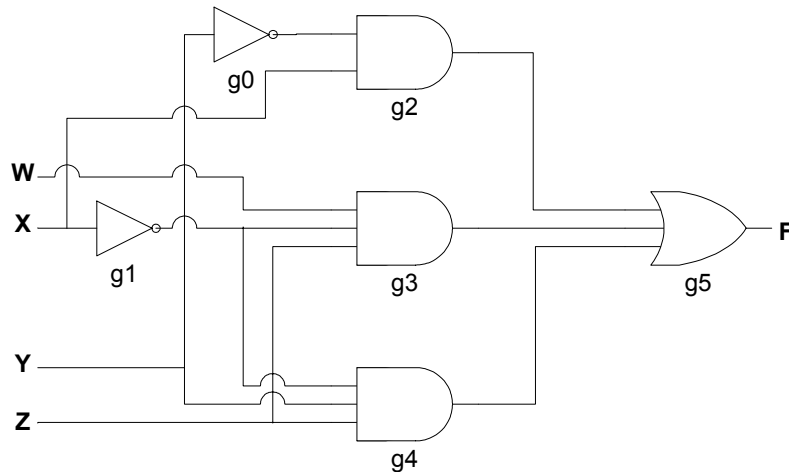
(e: 6 pts) Add one “don’t care” to the above function, as follows:

$$F = \sum_{w,x,y,z}(0, 4, 6, 7, 8, 9, 10, 11, 12, 13, 15) + d(14)$$

In this case, is the minimal S.O.P equal to the minimal P.O.S for F?
Briefly state why.

5. (21 Points Total) Consider the circuit below, which implements the following function:

$$F = \sum_{W,X,Y,Z}(3, 4, 5, 9, 11, 12, 13)$$



(a: 4 pts) Find all input combinations under which this circuit has a static hazard.

(b: 3 pts) Is this a static-0 or a static-1 hazard?

(c: 3 pts) Draw the additional gate(s) necessary in the circuit above to make sure that the circuit will not glitch.

(d: 3 pts) Given that the rising and falling propagation delay of each gate $g_0 - g_5$ is 1ns, what is the transition direction ($0 \rightarrow 1$ or $1 \rightarrow 0$) that causes the glitch?

(e: 4 pts) You present your solution to your boss, but he does not want to spend the money for any additional gates in the circuit. Instead, he tells you to fix the circuit by changing the rising and falling propagation delays of gates g_1 , g_2 , and/or g_3 . Write the inequalities in terms of $t_{pLH}^{g_1}$, $t_{pHL}^{g_1}$, $t_{pLH}^{g_2}$, $t_{pHL}^{g_2}$, $t_{pLH}^{g_3}$, $t_{pHL}^{g_3}$ that must be satisfied to ensure that the circuit does not glitch under any input transition.

(f: 4 pts) After spending a considerable amount of time on the above problem, your boss changes his mind and requests that you add one "don't care" to the function, such that its minimal S.O.P contains three prime implicants is hazard-free. In which cell of the K-map must you place the don't care; i.e:

$$F = \sum_{W,X,Y,Z}(3, 4, 5, 9, 11, 12, 13) + d(?)$$

(Show your K-map and circle the P.I.s used in the glitch-free implementation)

6. (15 Points Total) Consider a circuit that has three inputs i_2, i_1, i_0 and four outputs o_2, o_1, o_0 and ER. Let i_2, i_1, i_0 be the unsigned binary representation of the number $X = \{0-7\}$. For X in the range 0-4, the outputs o_2, o_1, o_0 should be the unsigned binary representation of $X+3$. For example, if $i_2 i_1 i_0 = 011$, then $o_2 o_1 o_0$ should be 110; if $i_2 i_1 i_0 = 001$, then $o_2 o_1 o_0$ should be 100, etc. For X equal to 5, 6, or 7, the output $o_2 o_1 o_0$ must be 000 and ER must be 1. In all other cases, ER must be 0.

Design this circuit using decoders, encoders, AND, OR, and NOT gates. Your implementation should only use four of the above components/gates.