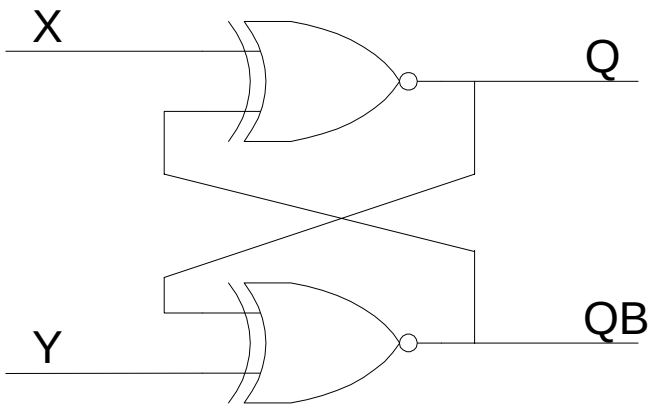
The University of Michigan
Department of Electrical Engineering and Computer Science

EECS 270 Fall 2002

Practice Exam #2 Solutions

Latches and Flip-Flops

1. Your manager was quite intrigued by your friend's (incorrect) SR-latch design, and decides to give it a try. He comes up with the following design:



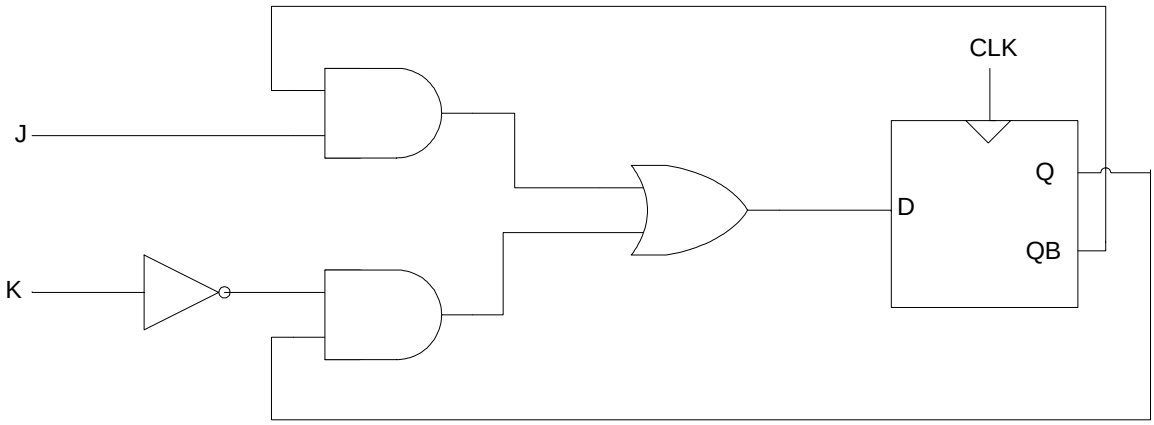
a) Fill in the truth table below:

X	Y	Q	QB
0	0	Last Q	Last QB
0	1	Oscillation	
1	0	Oscillation	
1	1	1/0 Non-deterministically	1/0

b) Is this circuit useful as a latch?

No. The latch behaves non-deterministically. There is also no way to set or reset this latch.

2. Derive the characteristic equation for the J-K flip-flop shown below.



D = J·QB + K'·Q

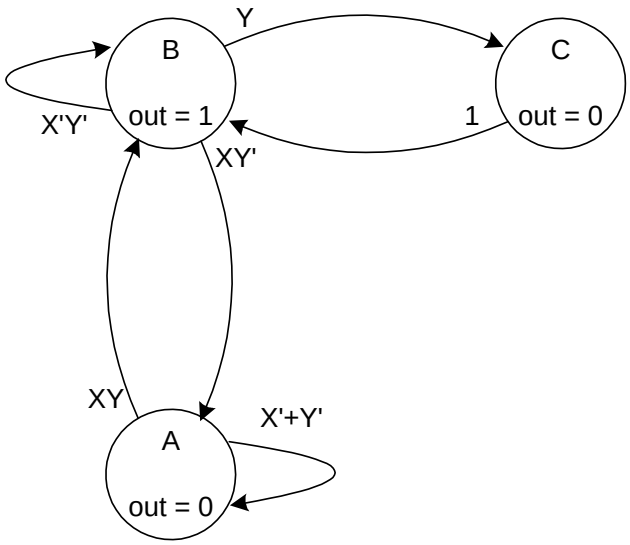
Characteristic Equation for D FF: Q* = D

Q* = D = J·QB + K'·Q

Q* = J·Q' + K'·Q

State Machine Analysis

3. Given the state machine described by the following state diagram:



a) Given the following state assignments, create the transition list and derive the minimal expressions for D1, D0 and out.

S	Q1	Q0
A	1	1
B	0	1
C	0	0

S	out	Q1 Q0	Transition Exp.	Q1* Q0* = D1 D0	S*
A	0	11	X' + Y'	11	A
A	0	11	XY	01	B
B	1	01	X'Y'	01	B
B	1	01	XY'	11	A
B	1	01	Y	00	C
C	0	00	1	01	B

D1 = Q1·Q0· (X'+Y') + Q1'·Q0·X·Y'
= Q1·Q0·X' + Q1·Q0·Y' + Q1'·Q0·X·Y'

(D0)' = Q1'·Q0·Y
D0 = Q1 + Q0' + Y'

out = Q1'·Q0

b) Assume that we cluster the unused state e = 10 with state A (i.e., state A = 1X). Derive the new minimal expression for D1.

Assign the transitions out of e to match those out of A:

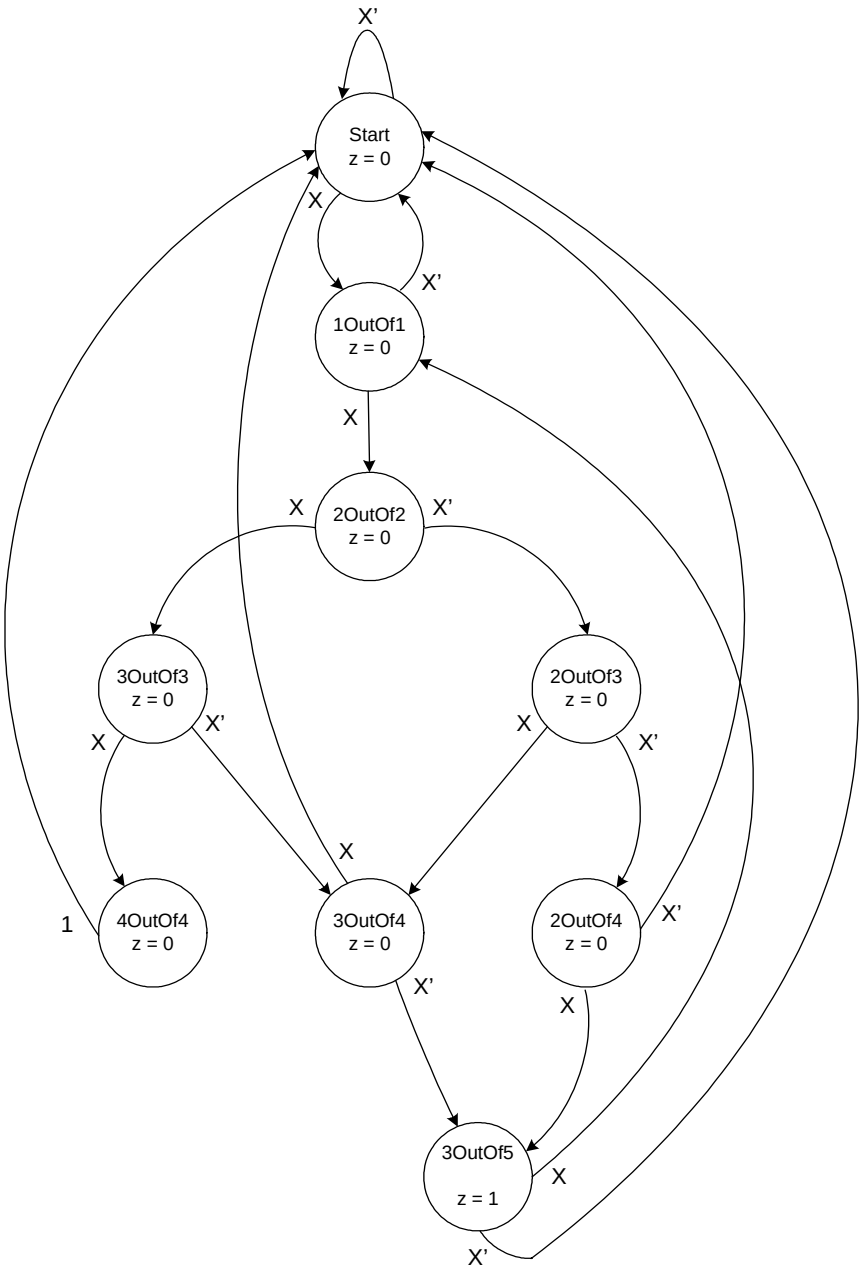
S	out	Q1 Q0	Transition Exp.	Q1* Q0* = D1 D0	S*
A	0	11	X' + Y'	11	A
A	0	11	XY	01	B
B	1	01	X'Y'	01	B
B	1	01	XY'	11	A
B	1	01	Y	00	C
C	0	00	1	01	B
e	0	10	X'+Y'	11	A
e	0	10	XY	01	B

D1 = Q1·Q0· (X'+Y') + Q1'·Q0·X·Y' + Q1·Q0'·(X'+Y')
= Q1·Q0·X' + Q1·Q0·Y' + Q1'·Q0·X·Y' + Q1·Q0'·X' + Q1·Q0'·Y'
= Q1·X' + Q1·Y' + Q1'·Q0·X·Y'

State Machine Design

4. Construct a state diagram for a one input, nine state machine which produces one (Moore-type) output z = 1 whenever the last string of five inputs contains exactly 3 1s **and** the string starts with 2 1s. After each string which starts with 2 1s, analysis of the next string will not start until the end of this 5 character string, whether it produces a 1 or not. For example, the input 11011010 produces an output of 00000000, whereas the input 10011010 produces 00000001

   Note: For this state diagram, the state name "XOutOfY" means that we have seen X ones out of Y bits so far in a given sequence.



Sequential Block Design

5. Construct a counter which produces the following sequence of numbers:

   1, 2, 2, 3, 3, 3, 4, 4, 4, 4, 5, 5, 5, 5, 5…15…15, 1, 2, 2, etc.
   (one 1) (two 2's) (three 3's) (four 4's) (five 5's)…(fifteen 15s) (one 1), etc.

   You can use counters that have load, enable, and reset inputs, and counters that can count up as well as down. Use only two counters and no more than 10 basic logic gates (nand, nor, and, or, inverter). *(It is possible for your design to use significantly less than 10 gates.)*

   Note: All counter inputs are active-high.