The University of Michigan
Department of Electrical Engineering and Computer Science

EECS 270 Fall 2003

Practice Final Exam

Name:_____ UM ID:_____

For all questions, show all work that leads to your answer.

Problem #	Possible Points	Points Earned
1	13	
2	19	
3	14	
4	17	
5	15	
6	12	
7	10	
Total	100	

I have neither given nor received any unauthorized aid on this exam.

Signed: _____

1. *Number Conversion: 13 Points Total*

(a: 3 pts) $-20_{10} = ?_2$ using a 6-bit two's-complement representation

(b: 3 pts) 11010_2 (two's-complement representation) = $?_2$ (one's-complement representation):

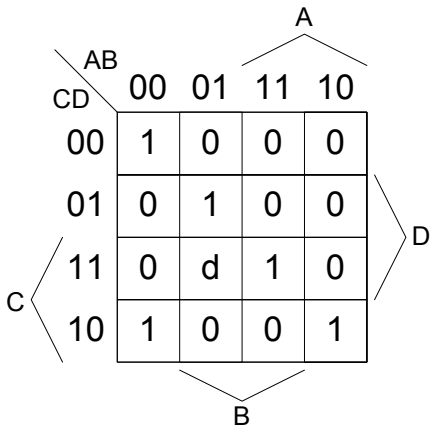
(c: 3 pts) $AB.9_{16} = ?_8$

(d: 4 pts) Represent the decimal number 26.6 with a binary number containing no more than eight bits. What is the numerical error in this representation of the number 26.6?

2. *K-Maps: 19 Total Points*

Consider the following function and its K-map:

$$F = \Sigma_{ABCD}(0, 2, 5, 10, 15) + d(7)$$



(a: 3 pts) Construct the minimal S.O.P. expression for F.

(b: 4 pts) Construct the minimal P.O.S. expression for F.

(c: 3 pts) What is the cost of each expression (S.O.P and P.O.S.) in terms of number of literals?

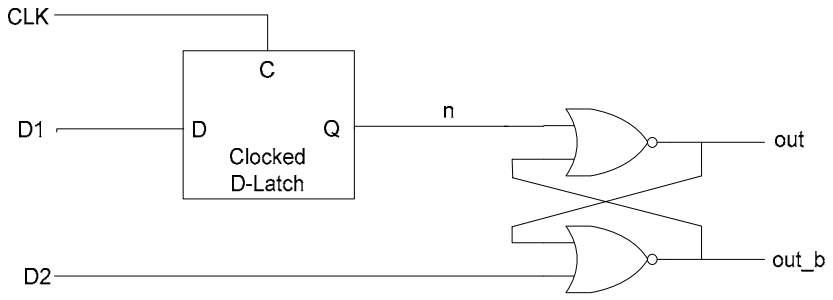
(d: 4 pts) Are the S.O.P. and P.O.S. identical functions?

.

(e: 5 pts) Change two cells in the K-map above to don't cares, and derive the new minimal S.O.P and P.O.S. expressions. Choose your don't cares such that:

1) The new minimal S.O.P. and P.O.S. are equal functions
2) The sum of the literals from the S.O.P. and P.O.S. is minimal.

3. *Sequential Circuits: 14 Total Points*



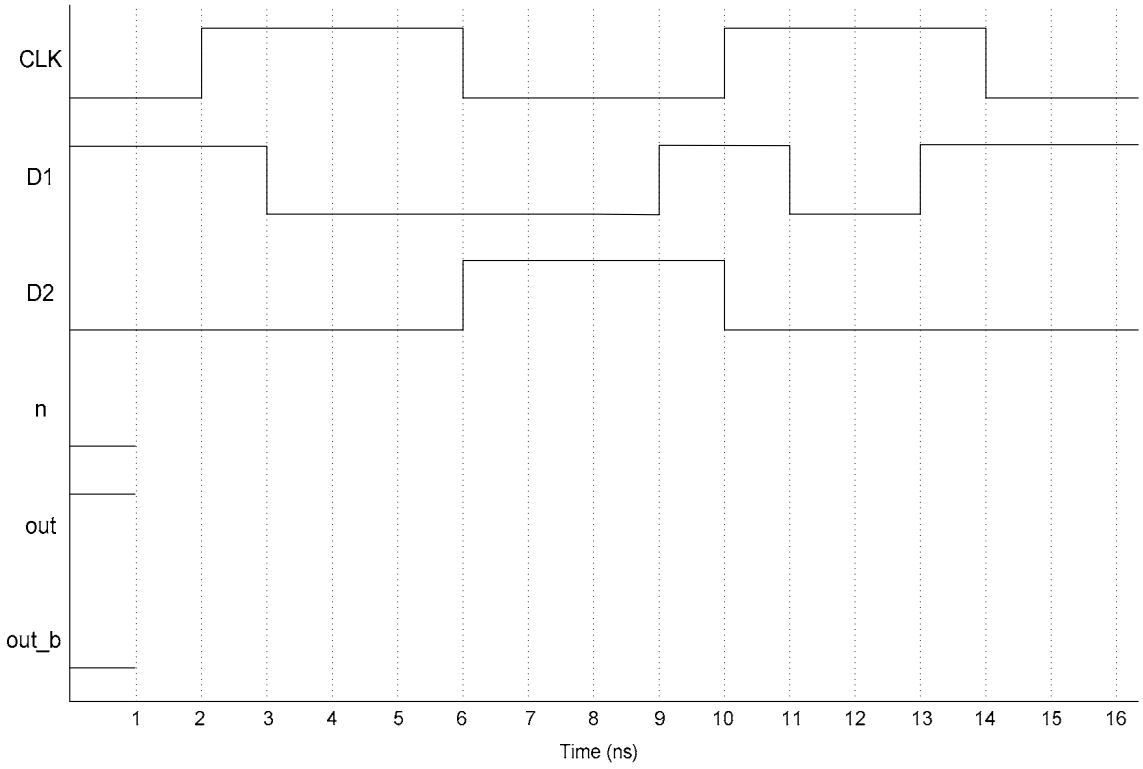
Given the circuit above, complete the timing diagram for signals n, out, and out_b. Assume that following values for the D-latch:

$$t_{setup} = t_{hold} = 1.5ns$$

$$t^{CQ}_{HL} = t^{CQ}_{LH} = 1ns$$

$$t^{DQ}_{HL} = t^{DQ}_{LH} = 2ns$$

Also, assume the NOR gates have a rising and falling delay of 1ns. Mark any regions of metastability with:



4. *State Machine Design: 17 Total Points*

Given a state machine with one input **x** and one output **Q**. Let *num_cyc_1* denote the number of previous clock cycles where **x** was a one and *num_cyc_0* denote the number of previous clock cycles where **x** was a zero. The state machine sets **Q** = 1 if (*num_cyc_1* - *num_cyc_0*) is a multiple of 3, i.e (*num_cyc_1* - *num_cyc_0*) = …-6, -3, 0, 3, 6… When the state machine starts, *num_cyc_0* and *num_cyc_1* are assumed to be zero.

Example sequence:

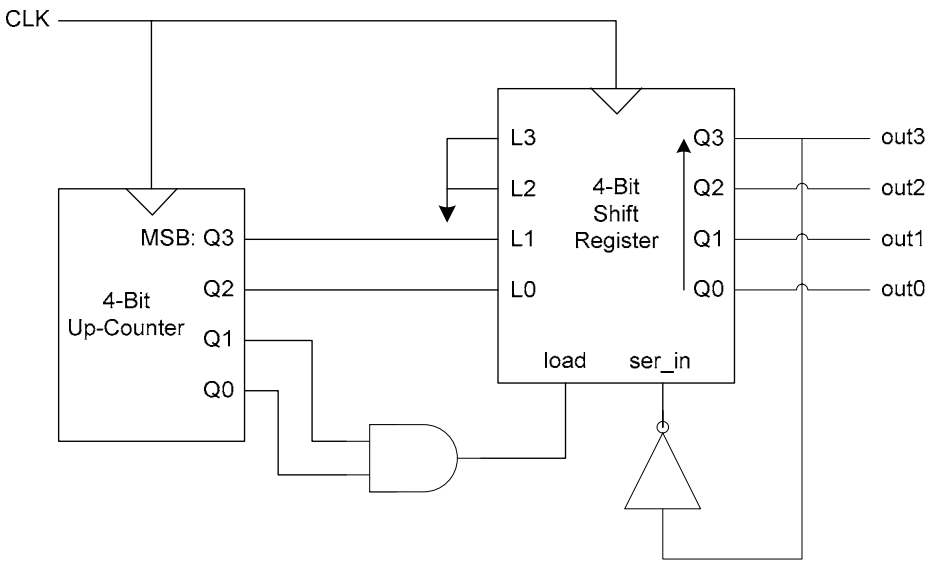
```
X:            100 001 110 101 110…
Q:            101 001 001 010 100…
num_cyc_0:    001 234 444 556 666…
num_cyc_1:    011 111 234 455 678…
```

Draw the state diagram for this state machine using no more than 5 states. Identify which state your machine should start in. Draw neatly and avoid crossing lines if possible.

5. *Counter/Shifter Design: 15 Total Points*

Consider the design on the next page, constructed with one “up” counter and one right/up shift register. Let outputs out3-out0 be the binary representation of a number *x* between 0 and 15 (out3 is the MSB). What is the repeating sequence of numbers *x* this design will produce?

Hint: Assume the counter starts in state Q3 – Q0 = 0011


CLK
MSB: Q3
Q2
Q1
Q0
4-Bit
Up-Counter
L3
L2
L1
L0
4-Bit
Shift
Register
Q3
Q2
Q1
Q0
load
ser_in
out3
out2
out1
out0

6. *Codes: 12 Total Points*

You have designed a system that transmits one of four 5-bit codes A, B, C, D, shown below, across a microwave link.

```
A:  0 1 1 0 0
B:  1 1 0 1 0
C:  1 0 1 0 1
D:  0 0 0 1 1
```

(a: 4 pts) What is the minimum Hamming distance of this code?

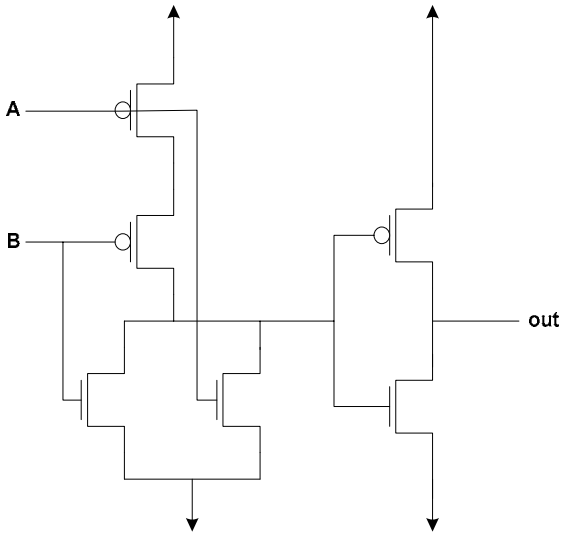
(b: 4 pts) Your manager explains to the customer that the microwave link is very robust and only a single bit in any 5-bit code can be flipped. If the data transmitted by the microwave link is corrupted and you receive the code X, shown below, can the received code be corrected? If yes, what was the transmitted code? If no, what is the set of possible transmitted codes?

X: 11101

(c: 4 pts) After buying your system, your customer finds that the microwave link is not quite as reliable as your manager had claimed. Your manager blames you for the problem and tells you to develop a solution, once again interrupting your latch design project. Upon investigation, you find that the link is such that either no bits are flipped in a transmitted code, or exactly two bits are flipped. Given this new information, can the code be corrected? If yes, what was the transmitted code? If no, what is the set of possible transmitted codes?

7. *CMOS: 10 Total Points*

(a: 5 pts) Given the circuit below, write out the Boolean equation for **out** as a function of inputs **A** and **B**.



(b: 5 pts) Is the gate shown below a valid CMOS gate? Briefly explain why or why not.