EECS 270 *Practice* final

Spring '04, Prof. Mark Brehob

Name: _____ UM ID: _____

Sign the honor code:

I have neither given nor received aid on this exam.

_____

Scores:

#	Points
1	/18
2	/25
3	/20
4	/15
5	/12
6	/10
Total	**/100**

NOTES:

- This exam is intended to be taken in 120 minutes.
- Throughout this exam * = AND, +=OR, !=NOT ⊕ = XOR
- Open book, open note.

1. Short answer **[18]**
    a. Using only 2-input AND, OR, and XOR gates as well as inverters draw a circuit which takes 6 bits as an input and outputs a 1 if the parity of those bits is odd. Label the inputs as I[0:5] and the output as "Odd_P". Your solution must have 8 or less gates (including the inverters). **[5]**

    b. Using only T flip-flops and standard gates, design a device which divides a clock by 8 and has a duty cycle of $1/8^{th}$. **[8]**

    c. Fill-in-the-blank **[5]**

        i. What is the clock frequency if the clock period is 20ns?
        _____

        ii. What is the difference between DRAM and SRAM?

        _____

        iii. Write the number 23_{16} as a binary number _____

        iv. Exactly how many ***bits*** of memory are in 1 Kbyte of RAM? provide a number (with no units)

        _____

        v. Write 10.01_2 as a base 10 number. _____

2. Consider a state machine that has one input (I) and one output (X). X is to go high whenever the last 4 values of "I" were "1010". An example input/output pair follows. **[25]**

```
I= 01010011001010100011
X= 00001000000001010000
```

   a. Is this a Mealy or Moore machine? Briefly explain. **[2]**

   b. Design a *state transition diagram* for this machine. **[13]**

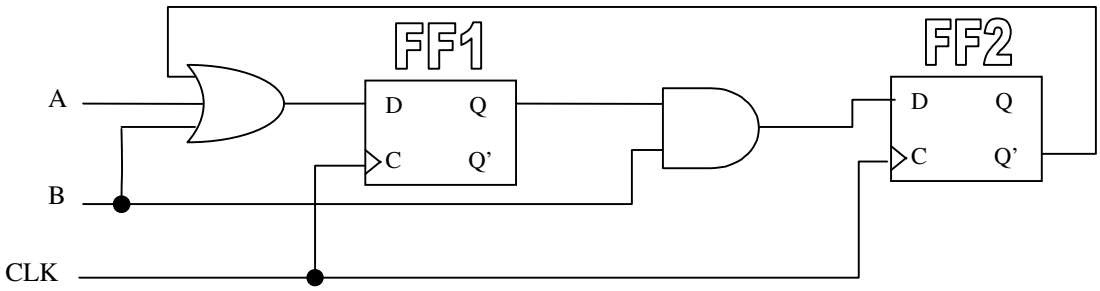
   c. Design the state machine using AND, OR, XOR and NOT gates (or inversion bubbles) and D flip-flops **[10]**

3. A circuit has three inputs and two outputs. The two inputs, I[1:0] represent the number N and I_1 is the most significant bit of that number. The two outputs, Z[1:0] are to be assigned as follows. If the current N is less than the previous N then Z_0=1. If the current N is greater than the previous N then Z_1=1. Otherwise Z_0=Z_1=1.
    a. Draw a Mealy state diagram which performs this task. Clearly label your states. **[10]**

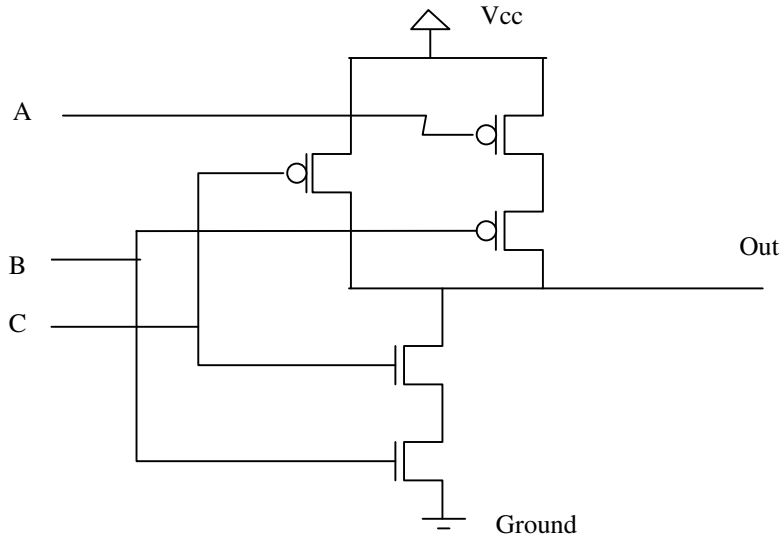
    b. Draw a Moore state-diagram which performs this task. Clearly label your states. **[10]**

4. MSI Logic and minimization **[15]**
   You are to find the minimal product-of-sums for a two-bit adder. The adder takes two 2-bit inputs (A[1:0] and B[1:0]) and generates a 2-bit output Z[1:0] and a carry-out bit Cout. A1, B1, and C1 are all the most significant bits. You are to use K-map(s) and clearly show your work.

5. Draw the state machine that corresponds to the following circuit. Label your states in terms of the flip-flops values in the order (Q1,Q2). Be sure to include all states. **[12]**



6. Fill in the following truth table with either “1”, “0” or “HiZ” **[10]**



A	B	C	Out
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	