Quiz 4 – EECS 270, Spring '04

Name: _____ unique name: _____

Honor code:
I have not given or received aid on this quiz, nor have I observed anyone else doing so:

Sign here:_____

This quiz is graded out of 30 points and is worth about 4% of your class grade. You will have **25** minutes for this quiz. ***Closed everything including calculators!*** To receive partial credit, work must be shown.

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1. Design a *Mealy* state transition diagram for the following problem. There are 2 inputs, X and Y, and one two-bit output M[1:0]. You are to output

   ((# of 1's in X since reset)+(# of 0's in Y since reset))mod 3

   The "mod 3" simply means to return the remainder when divided by 3. So if there had been 2 ones in X and 5 zeros in Y since reset the output would be one, or M[1:0]=01. The table below shows an example set of inputs and outputs. Just to be helpful, the value (# of 1's in X since reset)+(# of 0's in Y since reset) is listed under *sum* in the table. **[23]**

X	0	0	1	0	1	0	1	0	1
Y	1	0	1	1	0	0	1	1	0
Sum	*0*	*1*	*2*	*2*	*4*	*5*	*6*	*6*	*8*
M1	0	0	1	1	0	1	0	0	1
M0	0	1	0	0	1	0	0	0	0

   Be very sure that:
   - *It is clear which bits are inputs and which are outputs. Further that it is clear which bits are which.*
2. *You have indicated which state to start in.*

2. Using NMOS and PMOS transistors *only* design a three-input CMOS OR gate. **[7]**

3. Draw a D-**latch** using only ANDs, ORs, and NOTs (you may represent a NOT as a bubble, but you must do so clearly). **[7]**