EECS 373
Introduction to Embedded System Design

Robert Dick
University of Michigan

Lecture 12: Power

14 March 2024
Review

- Memory
- PCB design
Outline

- Power and energy
- Power integrity
Definitions

- Why? Power, temperature, energy, performance, and reliability important and deeply connected.
- Understand
  - why system failing and
  - why it consumes power.
- Temperature: Average kinetic energy of particle.
- Heat: Transfer of this energy.
  - Heat flows from regions of higher temperature to regions of lower temperature.
- Particles move.
- What happens to a moving particle in a lattice?
- Power: Rate of energy transfer (watts).
Why do wires get hot?

• Scattering of electrons due to destructive interference with waves in the lattice.
• What are these waves?
• What happens to the energy of these electrons?
• What happens when wires start very, very cool?
• What is electrical resistance?
• What is thermal resistance?
• Why do metals often have low thermal resistances?
Why do transistors get hot?

• Scattering of electrons due to destructive interference with waves in the lattice.
• Where do these waves come from?
• Where do the electrons come from?
  • Intrinsic carriers.
  • Dopants.
• What happens as the semiconductor heats up?
  • Carrier concentration increases.
  • Carrier mobility decreases.
  • Threshold voltage decreases.
Power consumption trends

- Initial optimization at transistor level.
- Further research-driven gains at this level difficult.
- Research moved to higher levels, e.g., RTL.
- Trade area for performance and performance for power.
- Clock frequency gains linear.
- Voltage scaling $V_{DD}^2$ – very important.
Power consumption

- \[ P = P_{\text{SWITCH}} + P_{\text{SHORT}} + P_{\text{LEAK}} \]
- \[ P_{\text{SWITCH}} = C \cdot V_{\text{DD}}^2 \cdot f \cdot A \]
- \[ P_{\text{SHORT}} = \frac{b}{12} \cdot (V_{\text{DD}} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t \]
- \[ P_{\text{LEAK}} = V_{\text{DD}} \cdot (I_{\text{SUB}} + I_{\text{GATE}} + I_{\text{JUNCTION}} + I_{\text{GIDL}}) \]
- \( C \): total switched capacitance
- \( V_{\text{DD}} \): high voltage
- \( f \): switching frequency
- \( A \): switching activity
- \( b \): MOS transistor gain
- \( V_T \): threshold voltage
- \( t \): rise/fall time of inputs
- \( \dagger \): PSHORT usually \( \leq 10\% \) of PSWITCH
- Smaller as \( V_{\text{DD}} \rightarrow V_T \)
DVFS

- Power drops superlinearly in V.
- Performance drops linearly in V.
- Double transistor count.
- Drop V.
- Drop f.
- Net result.
  - Reduced power.
  - Reduced energy, even though t increases.
- Fails when Vdd → Vth.
Typical control policies

• If utilization < ~80%, drop V, f.
• If utilization > ~80%, increase V, f.
• Latency: >100ms in some cases.
• Based on flawed assumption for interactive systems.

• If device has been used within X minutes, keep on.
• Otherwise, put in lower power management state.
Leakage paths

- Gate Leakage
- Subthreshold Leakage
- Junction Leakage
- GIDL Leakage
- Punchthrough Leakage
Subthreshold leakage

\[ I_{\text{subthreshold}} = A_s \frac{W}{L} v_T^2 \left(1 - \exp\left(-\frac{V_{DS}}{v_T}\right)\right) \cdot \exp\left(\frac{(V_{GS} - V_{th})}{n v_T}\right) \]

where \( A_s \) is a technology-dependent constant,
\( V_{th} \) is the threshold voltage,
\( L \) and \( W \) are the device effective channel length and width,
\( V_{GS} \) is the gate-to-source voltage,
n is the subthreshold swing coefficient for the transistor,
\( V_{DS} \) is the drain-to-source voltage, and
\( v_T \) is the thermal voltage.
Power, temperature, performance, and reliability

- Dynamic power consumption
  - Reduced frequency
  - Heat
  - Performance
  - Carrier mobility

- Leakage power consumption
  - Heat
  - Carrier concentration

- Battery depletion rate and electricity cost

- Process variation
  - Permanent faults
    - Wear
  - Transient faults
    - Dl/dt

- Severe wear

Power time series

- **Max Power**: Artificial code generating max CPU activity
- **Worst-case App Trace**: Practical applications worst-case
- **Thermal Power**: Running average of worst-case app power over a time period corresponding to thermal time constant
- **Average Power**: Long-term average of typical apps (minutes)
- **Transient Power**: Variability in power consumption for supply net
Energy

• Power integrated over time.
• Average power multiplied by time.
• $J$ (mA-h for batteries, multiplies by V).
State-based power modeling

• For each component.
  • For each state.
    • Sum time spent in state × average power for state.
• Time-dependent state transitions are central.
• Big eaters
  • Displays.
    • Fluorescent tubes.
    • OLEDs.
  • Wireless interfaces.
    • Cellular.
    • WiFi.
    • Bluetooth.
  • CPU.
# State-based power modeling

<table>
<thead>
<tr>
<th>Component</th>
<th>CPU</th>
<th>Wireless</th>
<th>Motor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power state</td>
<td>DFVS max 12W / 1%</td>
<td>Transmit 12W / 0.5%</td>
<td>On 20W / 2%</td>
</tr>
<tr>
<td></td>
<td>DVFS min 1W / 4%</td>
<td>Receive 10W / 10%</td>
<td>Off 0W / 98%</td>
</tr>
<tr>
<td></td>
<td>Sleep 1uW / 95%</td>
<td>Standby 1W / 39.5%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Off 0W / 0%</td>
<td>Off 0W / 50%</td>
<td></td>
</tr>
</tbody>
</table>

\[ A_{ps, dev} \text{ is the proportion of time } dev \text{ spends in } ps. \]
\[ P_{ps, dev} \text{ is the power consumption of } dev \text{ when in state } ps. \]
\[ P_{tot} = \sum_{ps \in \text{power states}} \sum_{dev \in \text{devices}} P_{ps, dev} \times A_{ps, dev} \]

This is extraordinarily useful, and of shocking simplicity.
Outline

- Power and energy
- **Power integrity**
Power integrity

• Why? Get it wrong and board resets itself or worse for no apparent reason.
A look at impedance
(with capacitors, inductors and resistors vs. frequency)

Notice the log scales!
Power integrity related faults

• Even short “power droops” cause failure.
• Stable power = power Integrity.
• Does C fix?
  – No: parasitics.
Non-ideal devices

- ESR is Effective Series Resistance
- ESL is Effective Series Inductance
- Ceff is the effective capacitance.
  - How does quantity effect these values?
- Obviously impedance will be varying by frequency.

<table>
<thead>
<tr>
<th>Device</th>
<th>Quantity</th>
<th>Cap</th>
<th>ESR</th>
<th>ESL</th>
<th>Ceff</th>
<th>ESR</th>
<th>ESL</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC/DC Converter</td>
<td>1</td>
<td>1.00E-04</td>
<td>7.00E-07</td>
<td></td>
<td>1.00E-04</td>
<td>7.00E-07</td>
<td></td>
</tr>
<tr>
<td>Tantalum Capacitors</td>
<td>3</td>
<td>3.30E-04</td>
<td>3.00E-02</td>
<td>3.00E-09</td>
<td>9.90E-04</td>
<td>1.00E-02</td>
<td>1.00E-09</td>
</tr>
<tr>
<td>0603 Ceramic Caps.</td>
<td>2</td>
<td>1.00E-06</td>
<td>3.00E-02</td>
<td>7.00E-10</td>
<td>2.00E-06</td>
<td>1.50E-02</td>
<td>3.50E-10</td>
</tr>
<tr>
<td>0603 Ceramic Caps.</td>
<td>8</td>
<td>1.00E-07</td>
<td>6.00E-02</td>
<td>6.00E-10</td>
<td>8.00E-07</td>
<td>7.50E-03</td>
<td>7.50E-11</td>
</tr>
<tr>
<td>0603 Ceramic Caps.</td>
<td>8</td>
<td>1.00E-08</td>
<td>9.00E-02</td>
<td>5.00E-10</td>
<td>8.00E-08</td>
<td>1.13E-02</td>
<td>6.25E-11</td>
</tr>
<tr>
<td>0603 Ceramic Caps.</td>
<td>10</td>
<td>1.00E-09</td>
<td>1.50E-01</td>
<td>5.00E-10</td>
<td>1.00E-08</td>
<td>1.50E-02</td>
<td>5.00E-11</td>
</tr>
<tr>
<td>PC Board</td>
<td>1</td>
<td>8.50E-08</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ESR/ESL contributors

- Bad solder jobs make ESR/ESL worse.
- Bad solder jobs make everything worse.
- **Everything.**
- Packaging has an impact.
- SMT eliminate wire parasitics.
- Pads can have an impact
Given the previous table
Removing the PCB

Decoupling Impedance vs Frequency

- Z(pup)
- Z(tant)
- Z(1uF)
- Z(0.1uF)
- Z(0.01uF)
- Z(pcb)
- ZT
- Z(LICA)
Staged capacitors

- Voltage regulator module
- Bulk bypass (tantalum) and decoupling capacitors (ceramic).
  - Instantaneous current.
  - Different frequencies.
- However sets of different capacitors cause problems!
Power integrity summary

• Use range of C values.
• Model frequency response.
  • Consider parasitics.
• SPICE works.
Other sources of information

  - **Very** nice tutorial/overview
  - Seems to have strong viewpoint
- http://www.goldengateographics.com/pcgloss.htm
  - Some definitions taken verbatim.
Done.