Low-Voltage Low-Power LVDS Drivers

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***Abstract*—Two low-voltage low-power LVDS drivers used for high-speed point-to-point links are discussed. While the previously reported LVDS drivers cannot operate with low-voltage supplies, the proposed double current sources (DCS) LVDS driver and the switchable current sources (SCS) LVDS driver are suitable for low-voltage applications. Although static current consumption is greater than the minimum amount required by the signal swing, the DCS LVDS driver is simple and fast. The SCS LVDS driver, by dynamically switching the current sources, draws minimum static current and reduces the power consumption by 60% compared to previously reported realizations. Both drivers were fabricated in a standard 0.35-μm CMOS process; they are compliant with LVDS standards and can operate at data rates up to gigabits-per-second.**

***Index Terms*—Back-plane drivers, fast data communication circuits, input/output (I/O) drivers, low-voltage differential signaling (LVDS), low-voltage low-power integrated circuits.**

I. Introduction

THE ever-increasing processing speed of microprocessor motherboards, optical transmission links, chip-to-chip communications, etc., is pushing the off-chip data rate into the gigabits-per-second range. While scaled CMOS technologies continue to enhance on-chip operating speeds, off-chip data rates have gained little benefit from the increased silicon integration. This is primarily due to the excessive power consumption necessary for driving impedance-controlled electrical interconnects, which leads to an increase in costs related to packaging and thermal management [1]. In the past, off-chip high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). Therefore, it is beneficial to move the off-chip data rate to the range of Gb/s-per-pin or above. Reducing the power consumption is also critical for battery-powered portable systems as well as some other systems in order to extend the battery life and reduce the costs related to packaging and additional cooling systems.

Scalable Coherent Interface (SCI) is a high-speed packet transmission protocol that efficiently provides the functionality of bus-like transactions (read, write, lock, etc.), but it uses a collection of fast point-to-point links instead of physical buses to reach higher speeds. The initial physical implementations were based on emitter coupled logic (ECL) signal levels [2], which consume more power than is practical in a low-cost workstation environment. Low-voltage differential signaling (LVDS) is a technology developed to provide a low-power and low-voltage alternative [3] to ECL and other high-speed I/O interfaces for point-to-point transmissions. LVDS achieves higher speed and significant power savings by means of a differential scheme for transmission and termination, in conjunction with low voltage swing.

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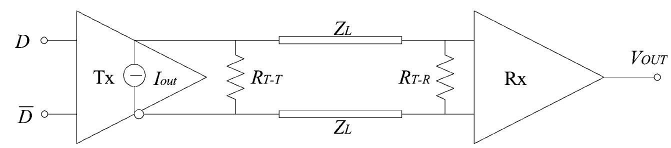

Fig. 1. LVDS interface with termination at the receiver and source ends for gigabits-per-second operation.

In this paper, two low-voltage, low-power, and high-speed LVDS drivers are discussed. Both drivers can operate with data rates of 1 Gb/s and above, and they are fully compatible with IEEE Std 1596.3-1996 [3] for general-purpose links and IEEE Draft P802.3ae/D5.0 [4] for XSBI interfaces. Section II discusses the LVDS interfaces, the typical LVDS drivers, and the design challenges for low-voltage operation. In Section III, the low-voltage, low-power LVDS drivers are discussed and some of the simulation results are also presented. The experimental results and conclusions are addressed in the last two sections.

II. Typical LVDS Drivers

An LVDS interface, as shown in Fig. 1, has a low-voltage swing (250–400 mV); it is connected point-to-point and achieves very high data rates (up to 500 Mb/s per signal pair) and reduced power dissipation [3]. LVDS uses differential data transmission and the transmitter is configured as a switched-polarity current generator. A differential load resistor at the receiver end provides optimum line impedance matching.

Due to the imperfect termination, package parasitics, component tolerances or crosstalk [5], there are reflected waveforms returning to the driver. As data rates push significantly above 500 Mb/s and connectors are added, an additional termination resistor is usually placed at the source end to suppress reflected waves, and the LVDS signaling can be substantially enhanced. Low voltage differential signaling is a standardized data transmission format that is widely used for serial data transmissions; as shown in Fig. 2, a differential signal is centered at a common-mode voltage of about 1.25 V. The maximum magnitude of the differential signal is 400 mV. Typically, the LVDS signal varies in magnitude from 1.05 to 1.45 V.

A typical bridged-switches LVDS driver behaves as a current source with switched polarity as shown in Fig. 3(a) [3]. The bias current I_b is switched through the termination resistors according to the data input, and thus produces the correct

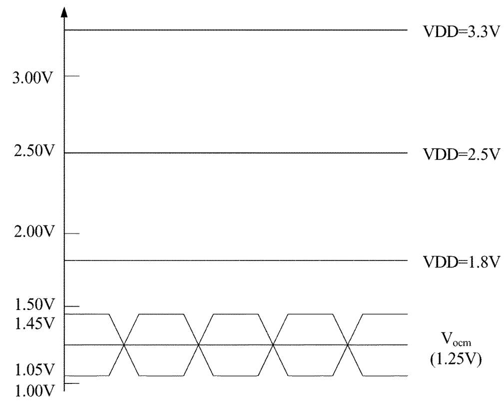

Fig. 2. LVDS signal formatting.

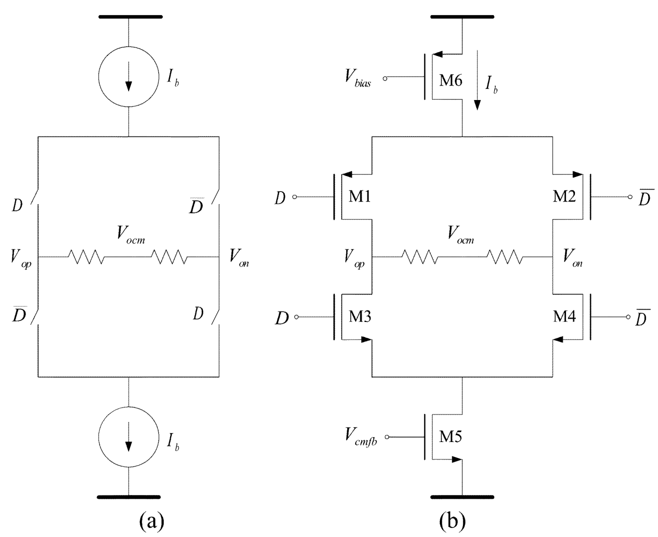

Fig. 3. Typical LVDS driver: (a) macromodel and (b) transistor implementation [3].

differential output signal swing. A possible implementation of the typical LVDS driver is shown in Fig. 3(b). It uses four MOS switches (M1–M4) in a bridged configuration. If switches M1 and M4 are on $(D = \text{LOW})$, the polarity of the output current is positive together with the differential output voltage. On the contrary, if switches M1 and M4 are off (switches M2 and M3 are on), the polarity of the output current and voltage is reversed.

The typical LVDS driver works well if the supply voltage (V_{DD}) is 2.5 V or greater. It is simple and only needs minimum static current consumption to produce the required output signal swing. But when the supply voltage drops below 2 V (e.g., 1.8 V for 0.18-μm CMOS technology), the typical LVDS driver does not have enough headroom in the V_{DD} direction. This is mainly due to the finite on-resistance of the PMOS transistor switches and the large amount of current (nominally 6.4 mA for a signal swing of 320 mV and a 50-Ω termination resistance) flowing through the switches. The voltage drop across the transistor consumes headroom and it demands relatively high voltage supplies for the LVDS driver to operate properly.

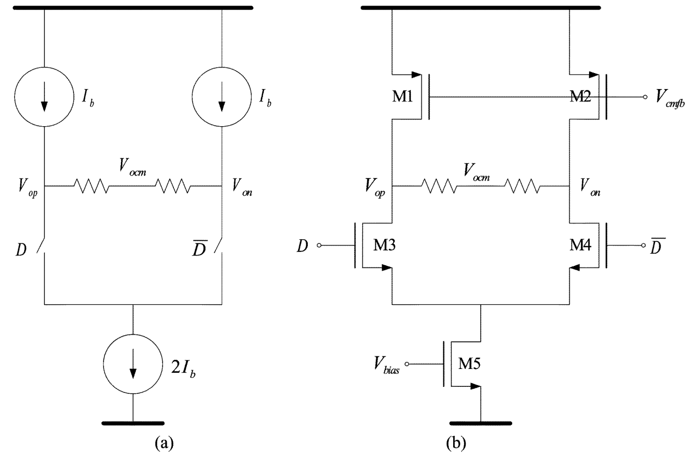

Fig. 4. DCS LVDS driver. (a) Model and (b) potential transistor level realization.

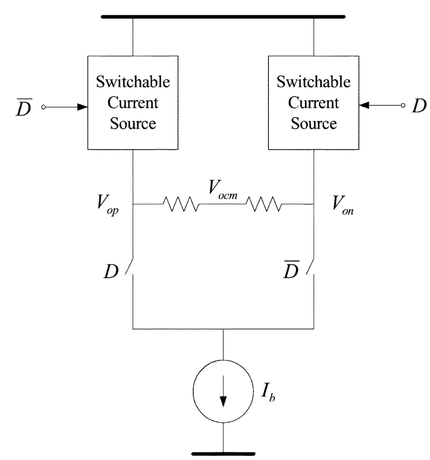

Fig. 5. SCS LVDS driver model.

III. Low-Voltage, Low-Power LVDS Drivers

A. Double Current Sources (DCS) LVDS Driver

A solution to the headroom issue discussed in Section II is to remove the top PMOS switches in the typical LVDS driver [Fig. 3(b)] and replace them by two PMOS current sources, as shown in Fig. 4(a); We call this structure a double current sources (DCS) LVDS driver. In order to produce the same signal swing, the bottom NMOS current source is required to sink $2I_b$, which doubles the static current consumption as required by the output signal swing. Accordingly, the embodiment of Fig. 4(b) consumes more current than the embodiment of Fig. 3(b). In addition, the NMOS transistor switches and the bottom NMOS current source are required to be larger than the corresponding transistors in Fig. 3(b). If an integrated circuit includes a plurality of LVDS drivers, the increased current consumption and transistor dimensions may limit their applications. Also, larger transistor dimensions increase the total pad capacitance and so reduce the pin bandwidth.

B. Switchable Current Sources (SCS) LVDS Driver

Another solution to the headroom issue is shown in Fig. 5. Instead of using two constant current sources at the top, two switchable current sources are used [6]. Depending on the data input, one of the two switchable current sources will

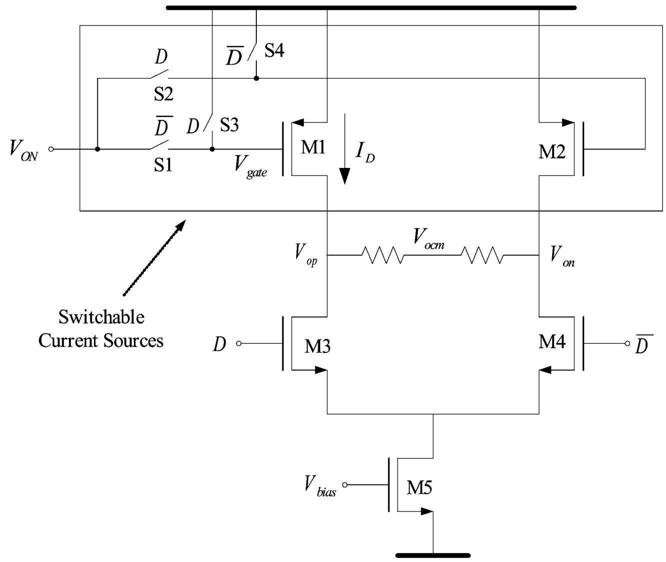

Fig. 6. SCS LVDS driver with control circuit.

conduct current. This current flows through the termination resistors and produces the output voltage swing. Notice that the bottom NMOS current source only needs to sink I_b, leading to minimum static current consumption.

Fig. 6 shows the basic principle behind the proposed SCS LVDS driver. When $V_{\rm ON}$, a reference voltage, is applied to the gate of M1(M2), the transistor conducts a current I_D, which is a copy of a well-controlled reference current, regardless of the process, voltage, and temperature (PVT) variations. Here, transistors M1 and M2 and switches S1, S2, S3, and S4 act as switchable current sources. For instance, when D is LOW (M1 is ON) then M1 conducts current I_D, and it flows throughout the load resistors and M4 to produce the proper output voltage swing.

There are two design issues that need to be addressed for the SCS LVDS driver to operate properly. First, we must determine how to generate the reference voltage $V_{\rm ON}$ such that I_D remains at the proper value regardless of the PVT variations. Second, since the PMOS switchable current sources need to conduct large currents, their transistor dimensions are large as well as their parasitic capacitances. So the question is either how to switch the gate voltages of M1 and M2, or how to quickly charge and discharge the parasitic capacitors at the gates of M1 and M2. The design issues mentioned above are addressed in the SCS LVDS driver shown in Fig. 7; its operation is explained as follows.

The SCS LVDS driver contains two parts: the switchable current source control module and the core of the LVDS driver. The left part of Fig. 7 is the control module, and it is used to generate $V_{\rm ON}$ such that when it is applied to the gate of M1(M2) its drain current I_D is proportional to $I_{\rm ref}$. The cascode transistor M7 and amplifier Amp form a regulated-gain control (RGC) loop. This RGC loop is used to set M6's drain voltage to $V_{D\_{\rm ref}}(= 1.41\ {\rm V})$. It is important to make sure that the output common-mode voltage and signal swing are maintained; hence the higher output voltage of $V_{\rm op}(V_{\rm on})$ is fixed, and it is defined by $V_{D\_{\rm ref}}(= V_{\rm ocm\_ref} + V_{o,{\rm swing}}/2)$, regardless of the PVT variations. $V_{\rm ocm\_ref}$ is the output common-mode reference voltage, and $V_{o,{\rm swing}}$ is the required signal swing. For instance, for an output common-mode voltage of 1.25 V and an output signal swing of 320 mV, ideally the higher LVDS output voltage $V_{\rm op}(V_{\rm on})$ should be 1.41 V. By setting the drain voltage of M6 to $V_{D\_{\rm ref}}$, we have good matching for the current mirror composed of M6 and M1 (M2). Another issue worth mentioning is that the switchable current source control module can be shared by several LVDS drivers, but independent buffers are used for each driver in order to minimize the signal feedthrough.

The right part of Fig. 7 is the core of the SCS LVDS driver. The switchable current sources are used to generate current I_D and they are composed of transistors M1 and M2, buffer-connected amplifier Buf-A, switches S1 and S2, and the pull up/down circuits. The pull up/down circuits are used to quickly change the gate voltages of M1 and M2, i.e., to quickly charge or discharge the parasitic capacitors associated with the node $V_{\rm gate}$. The buffer-connected amplifier Buf-A is used to isolate the DC voltage $V_{\rm ON}$ from the data controlled switches. It also provides "fine adjustment" to the gate voltage of M1(M2) when the switch S1(S2) is closed, while the pull up/down circuit, driven by the input data, provides coarse control. The CMFB is used to set the output common-mode voltage to the desired reference voltage $V_{\rm ocm\_ref}$.

The operation of the switchable current sources is explained as follows. If data D is LOW, then switch S1 is ON and switch S2 is OFF. The M1's gate voltage is pulled down to $V_{\rm ON}$ through the pull up/down circuit during the data transition while M2's gate voltage is pulled up close to V_{DD}. M1 conducts current I_D and M2 is OFF. The current I_D flows through the termination resistors and produces the signal swing.

C. Pull Up/Down Circuits

An active pull up/down circuit is shown in Fig. 8 [7]. In this structure, both pull up and pull down sections produce short periods of current pulses at the data's transition edges. These current pulses are used to charge/discharge the parasitic capacitors and so to pull up/down the switchable current source gate voltages. Some design issues are associated with this active pull up/down circuit. First, the circuit itself consumes huge dynamic power since the several delay cells used and the high data rate. Second, the currents produced by the pull up/down circuit are finite and they limit the speed of the charging/discharging process. Also, since the currents are produced by PMOS and NMOS transistors, respectively, the charge injected into the capacitors may not equal the charge extracted from the capacitors. This difference should be supplied by the "Buffer" as shown in Fig. 7, and this requires a fast circuit implementation that demands more power consumption.

Instead of using an active pull up/down circuit, we propose to use passive capacitors C_{PP} driven by the input data for the SCS LVDS driver; the principle of operation is shown in Fig. 9. The passive pull up/down circuit does not have the drawbacks faced by the active pull up/down circuit mentioned above. The capacitor C_{PP}, driven by the input data D, is used to pull up/down M1(M2) gate voltage with drastically reduced transition time and to provide coarse control over the gate voltage $V_{\rm gate}$. The parasitic capacitor C_P associated with the node $V_{\rm gate}$, and capacitor C_{PP} form a capacitive voltage divider. When D goes

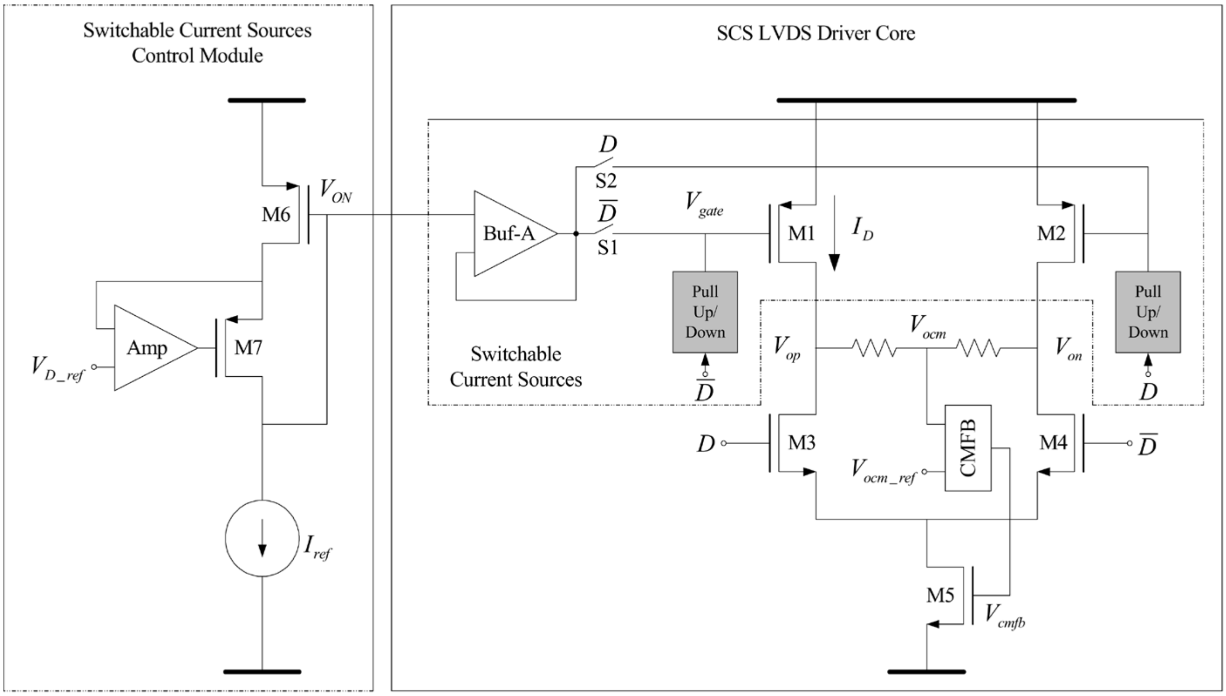

Fig. 7. SCS LVDS driver with active pull up/down circuit auxiliary circuits.

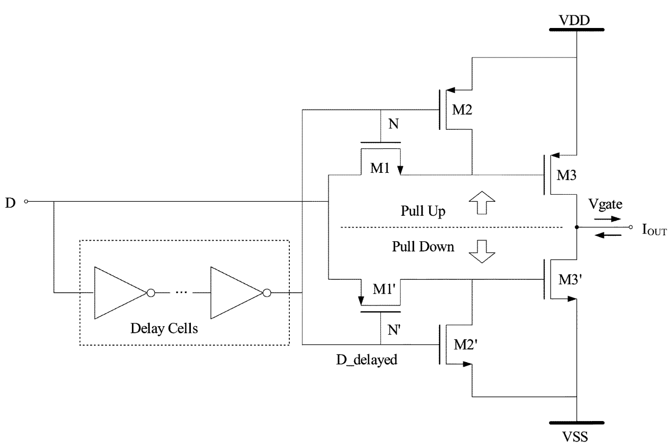

Fig. 8. Active pull up/down circuit [7].

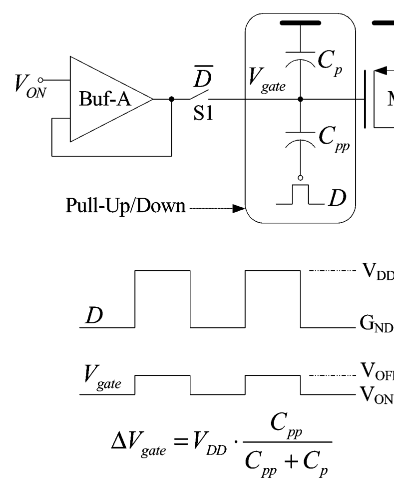

Fig. 9. Passive pull up/down circuit based on charge redistribution.

down, $V_{\rm gate}$ equals $V_{\rm ON}$ and I_D is determined by $I_{\rm ref}$, while C_{PP} is charged to $V_{\rm ON}$. During the low-high transition of D, the switch resistance is high and the C_{PP}'s injected charge is mainly absorbed by C_P, turning off the transistor. The resulting waveforms of the data and the gate voltage $V_{\rm gate}$ are also shown in Fig. 9. It is easy to show that the M1(M2) gate voltage variation $\Delta V_{\rm gate}$ can be expressed as

$$\Delta V_{\rm gate} = \frac{C_{pp}}{C_{pp}+C_p}\cdot V_{DD} \tag{1}$$

where $\Delta V_{\rm gate}$ is defined as $\Delta V_{\rm gate} = V_{\rm OFF} - V_{\rm ON}$. It is assumed that data D varies from V_{DD} to zero.

It is worth mentioning that when the transistor M1 (M2) is turned off, its gate voltage $V_{\rm OFF}$ does not need to be V_{DD}; for fast circuits, it is better for $V_{\rm OFF}$ to be lower than V_{DD} such that the transistor operates in subthreshold region. In this way, we can turn on/off the switchable current sources more quickly and minimize the dynamic power consumption needed to charge/discharge C_{pp} and C_p, as long as the current flowing through the OFF switchable current source $I_{\rm OFF}$ is negligible.

By choosing a proper limit for $I_{\rm OFF}$, we can find the gate voltage variation $\Delta V_{\rm gate}$ such that $I_{\rm OFF}$ does not exceed this limit. Then, the value of the capacitor C_{pp} can be determined as

$$C_{pp} = \frac{C_p \cdot \Delta V_{\rm gate}}{V_{DD} - \Delta V_{\rm gate}}. \tag{2}$$

For this design, C_p is around 6.4 pF and C_{pp} is chosen to be 0.8 pF, which occupies 1000 μm^2 with poly-poly implementation. The switches are implemented with transmission gates; transistor dimensions are 60/0.4 and 20/0.4 for PMOS and NMOS, respectively. The current flowing through the OFF switchable current source $I_{\rm OFF}$ is around 240 μA and $\Delta V_{\rm gate}$ is around 200 mV. Notice that the data D drives an equivalent

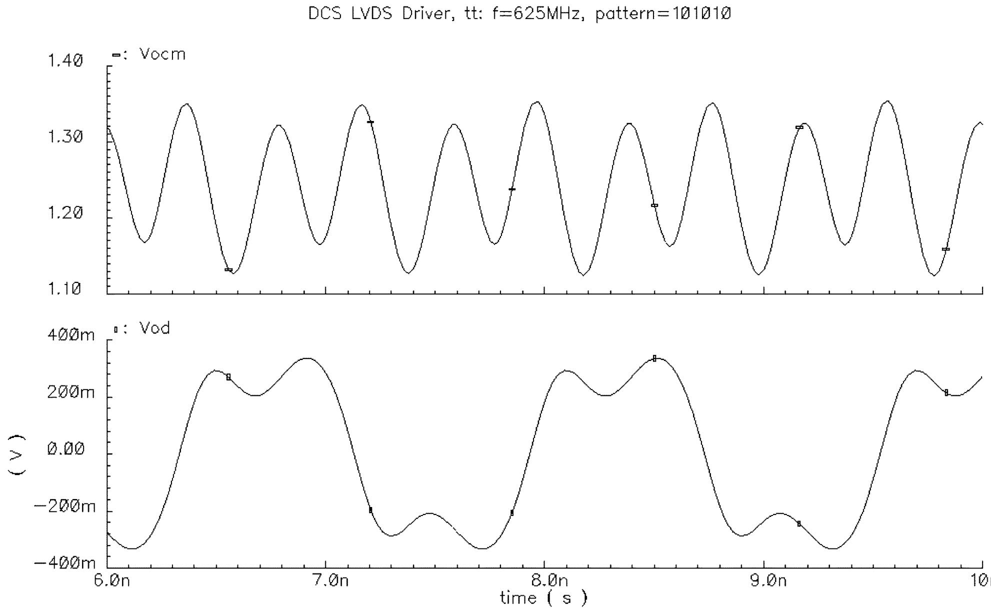

Fig. 10. Common-mode and differential-mode DCS LVDS driver output waveforms with load model.

capacitance of approximately 0.7 pF; hence D and $\overline{D}$ are not severely affected by the pull up/down capacitor C_{pp}.

When the switchable current source M1 (M2) is turned on, the pull up/down capacitor C_{pp} is connected to ground (logic ZERO); so it is important to reduce the substrate noise to minimize its effect on the output signal amplitude. When M1 (M2) is turned off, C_{pp} is connected to the power supply (logic ONE). Since M1 (M2) is working in the subthreshold region, its current is very small hence the supply variation has very limited effect on the output signal amplitude.

Compared to the active pull up/down circuit, this passive pull up/down circuit is faster as a result of the capacitors used, consumes less power, and the up/down voltage changes are symmetrical. With symmetrical voltage changes, the switches S1 and S2 can be small and the speed of the Buf-A is relaxed. Also, the driver's architecture is simpler and, therefore, more robust.

D. Simulation Results

The transistor dimensions of the DCS and SCS LVDS driver cores are shown in Table I. The simulated DCS LVDS driver output common-mode and differential-mode voltages with data rate of 1.25 Gb/s are shown in Fig. 10. In this simulation, the models of the electrical static discharge (ESD) device, bonding wire, and package are included. Also, the termination resistor and load capacitors at the receiver end are included. Notice that both common-mode and differential-mode output voltages are within the LVDS standard specifications.

From the discussions in the aforementioned sections, it can be seen that the key design issue of the SCS LVDS driver is to control the switchable current source gate voltage $V_{\rm gate}$ and so the corresponding drain current. Fig. 11 shows the simulation results for the switchable current source gate voltage $V_{\rm gate}$ (top trace), transistor drain current I_D (middle trace) and the corresponding output differential voltage (bottom trace); the load model was simplified in order to see $V_{\rm gate}$ change more clearly. Notice that the gate voltage $V_{\rm gate}$ and the corresponding drain

TABLE I
TRANSISTOR DIMENSIONS OF THE DCS AND SCS LVDS CORES

Transistor	M1=M2	M3=M4	M5
DCS LVDS W/L (μm/μm)	4000/.4	600/.4	2000/.4
SCS LVDS W/L (μm/μm)	4000/.4	200/.4	1000/.4

current I_D switches properly. The transition time is only around 240 ps and it can be seen that the rising time and falling time of the output signal are within the specifications (300–500 ps). The small transition time is mainly due to the passive capacitors used for the pull up/down circuit, and operating the switchable current sources in a subthreshold region when they are turned OFF. The gate voltage variation $\Delta V_{\rm gate}$ is around 200 mV, and the drain current $I_{\rm ON}$ and $I_{\rm OFF}$ are around 6.4 mA and 240 μA, respectively. Notice that the gate voltage $V_{\rm gate}$ and the drain current I_D present small variations. They are due to the transients of charging/discharging the parasitic capacitances.

IV. EXPERIMENTAL RESULTS

Both the DCS and SCS LVDS drivers have been fabricated in the TSMC 0.35-μm CMOS process through the MOSIS service; the active die areas are 0.11 mm^2 and 0.14 mm^2, respectively. The chip micrograph is shown in Fig. 12 and was packaged in a 64-pin ceramic quad flat package. According to the experimental results, the DCS LVDS driver operates properly for a data rate up to 1.4 Gb/s and the SCS LVDS driver operates for data rates up to 1.2 Gb/s. Those shortcomings might be alleviated if more advanced processes or N-type switchable current sources are used.

Figs. 13 and 14 show the DCS LVDS driver differential output eye diagrams with $2^{31}-1$ pseudorandom bit sequence (PRBS) pattern and data rates of 680 Mb/s and 1.0 Gb/s, respectively. The single-ended output signal swings are around 340 mV and

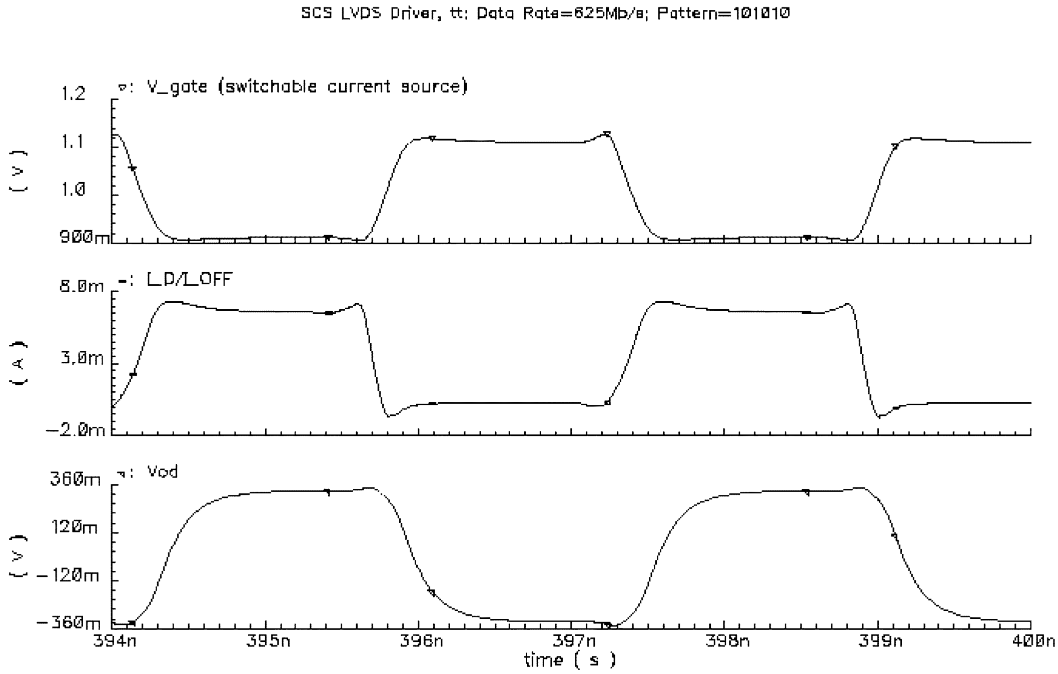

Fig. 11. Switchable current source gate voltage (top), drain current (middle), and the output differential voltage (bottom).

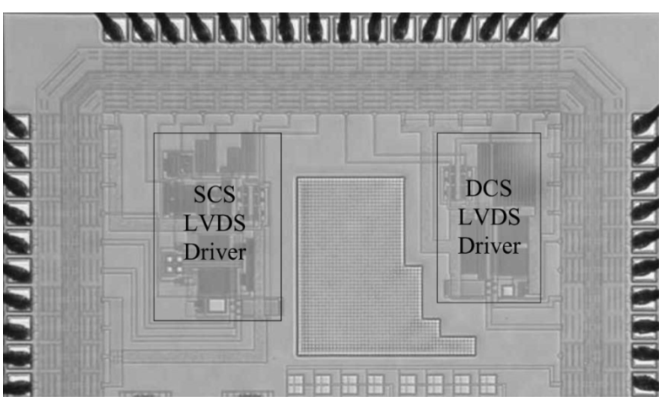

Fig. 12. DCS and SCS LVDS drivers chip micrograph.

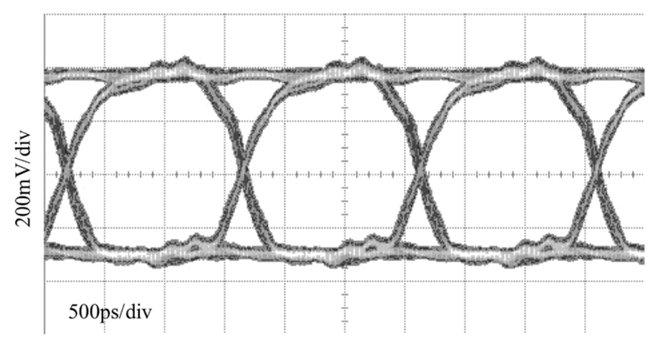

Fig. 13. DCS LVDS driver eye diagram (data rate = 680 Mb/s).

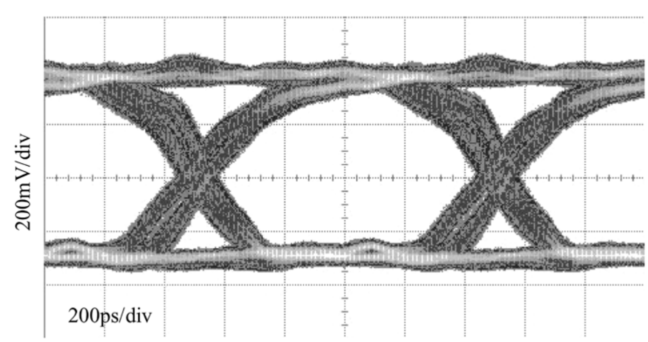

Fig. 14. DCS LVDS driver eye diagram (data rate = 1.0 Gb/s).

the measured root-mean-square (RMS) jitters are 15 and 36 ps, respectively. The eye openings are 90% and 80%, respectively. Figs. 15 and 16 show the SCS LVDS driver differential eye diagram with $2^{31}-1$ PRBS at data rates of 680 Mb/s and 1.0 Gb/s, respectively. The differential output signal swings are 680 mV and the measured RMS jitters are 28 and 50 ps, respectively. The eye openings are 85% and 60%, respectively.

Compared to the DCS LVDS driver, the SCS LVDS driver presents larger jitter and narrower open eyes. Several factors contribute to this. First, the rising and falling times of the SCS LVDS driver output signal are larger than those of the DCS LVDS driver output signal, which is due to the finite transition times of the gate voltage and drain current of the switchable current sources. Second, while the drain current of the PMOS current sources in the DCS LVDS driver remains constant, the drain current of the switchable current sources presents some variations, which is due to the transients of charging/discharging the parasitic capacitances. Also, the effect of the charge injection on the driver's output nodes is more pronounced for the SCS LVDS driver than for the DCS LVDS driver.

The total current consumption (including both static and dynamic) of the two LVDS structures for different data rates are given in Table II. The dynamic power consumed by the parasitic capacitance of the NMOS switches has been neglected for both structures. While in this table the current consumption of the DCS LVDS driver only consists the static tail current, that of the

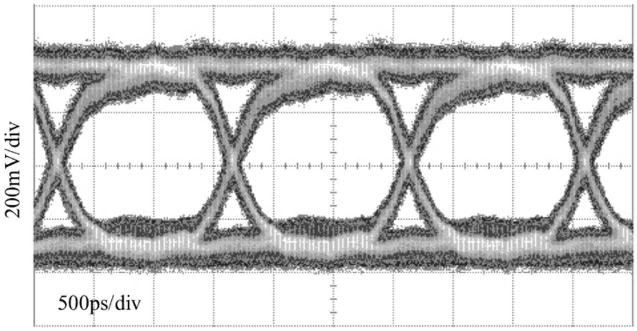

Fig. 15. SCS LVDS driver eye diagram (data rate = 680 Mb/s).

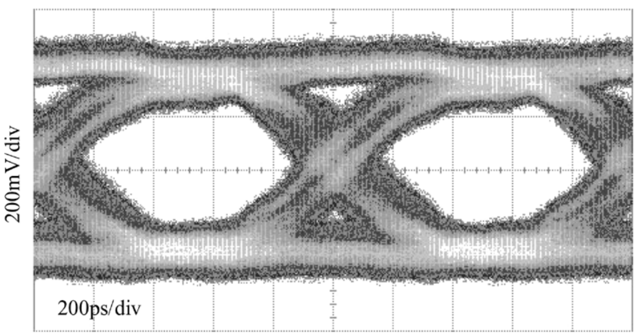

Fig. 16. SCS LVDS driver eye diagram (data rate = 1.0 Gb/s).

TABLE II
CURRENT CONSUMPTION FOR DCS AND SCS LVDS DRIVERS

Data Rate (Mb/s)	680	1000
DCS $I_{average}$ (mA)	12.8	12.8
SCS $I_{average}$ (mA)	8.5	9.0

TABLE III
COMPARISON WITH PREVIOUS REALIZATIONS

	[8]	DCS	SCS
Technology	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS
Output Voltage Swing (mV)	412	340	340
Maximum Data Rate (Mb/s)	1200	1400	1200
Static Power Consumption (mW)	43	23	12.8
Cell Size (mm^2)	0.17	0.11	0.14
Supply Voltage (V)	3.3	1.8	1.8

SCS LVDS driver includes the current drawn by the buffer-connected amplifier Buf-A, the dynamic current consumed by the parasitic capacitance of the switchable current sources, and the static tail current. It can be seen that the SCS LVDS driver draws much less current than the DCS LVDS driver.

A comparison among these two structures and a previously reported LVDS driver [8] is shown in Table III. This reported driver is based on typical LVDS configurations, except that it uses all NMOS switches to reduce the charge injection effects. Another reported LVDS driver requires an external resistor and two reference voltages [9]. Notice that both the DCS and SCS LVDS drivers consume less power than previous realizations. Especially for the SCS LVDS driver, by dynamically switching the current sources, it reduces the power consumption by 60% compared to the previous implementations (if the same signal swing is maintained). In addition, while the previously reported LVDS drivers cannot operate properly with low-voltage supplies, both the DCS and SCS LVDS drivers are suitable for low-voltage supply applications, and they are still compliant to LVDS standards and operate properly at very high data rates.

In addition to the low-power consumption, the other benefits of the low-voltage supply drivers are reduced EMI and costs related to the packaging and cooling systems. Being able to operate with low-voltage supplies makes it possible to use the same supply for both the core circuits and the I/O drivers, which can simplify both circuit and PCB design.

V. CONCLUSION

Two LVDS driver structures suitable for very low-voltage supplies (as low as 1.8 V) are discussed. The DCS LVDS driver is simple and fast. Despite the dynamic power consumed by the parasitic capacitance of NMOS switches, the DCS LVDS driver power consumption is almost constant, regardless of the data patterns. A drawback of the DCS LVDS driver is that its static current consumption is twice the minimum required by the output voltage swing. Another drawback is that the transistor dimension of the switches and the bottom NMOS current sources are relatively large because of the larger amount of current used, therefore die area and parasitic capacitors increase.

The SCS LVDS driver is more complex compared to the DCS LVDS driver, but its most significant advantage is that the static current consumption is kept to the minimum as required by the output voltage swing and load. Since it is needed to charge/discharge the parasitic capacitance associated with the switchable current sources, the SCS LVDS driver power consumption depends on the data pattern, even if we neglect the dynamic power consumed by the parasitic capacitance of NMOS switches. The higher the data rate, the larger the dynamic power consumption of the pull up/down circuit is.

REFERENCES

[1] R. A. Nordin, A. F. J. Levi, R. N. Nottenburg, J. O'Gorman, T. Tanbun-Ek, and R. A. Logan, "A systems perspective on digital interconnection technology," *J. Lightwave Technol.*, vol. 10, pp. 811–827, Jun. 1992.

[2] *F100K ECL 300 Series Data Book and Design Guide*, National Semiconductor Corp., 1992.

[3] *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), 1596.3 SCI-LVDS Standard*, IEEE Std 1596.3-1996, 1996.

[4] *IEEE Standard for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications-Media Access Control (MAC) Parameters, Physical Layer and Management Parameters for 10 Gb/s Operation*, IEEE Draft P802.3ae/D5.0, May 1, 2002.

[5] H. W. Johnson and M. Graham, *High-Speed Digital Design, A Handbook of Black Magic*. Englewood Cliffs, NJ: Prentice Hall, 1993.

[6] R. Senthinathan and J. L. Prince, "Application specific CMOS output driver circuit design techniques to reduce simultaneous switching noise," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1383–1388, Dec. 1993.

[7] Y. Ohtomo, M. Nogawa, and M. Ino, "A 2.6-Gbps/pin SIMOX-CMOS low-voltage-swing interface circuit," *IEICE Trans. Electron.*, vol. E79-C, no. 4, pp. 524–529, Apr. 1996.

[8] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-Pin operation in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 706–711, Apr. 2001.
[9] T. Gabara, W. Fisher, W. Werner, S. Siegel, M. Kothandaraman, P. Metz, and D. Gradl, "LVDS I/O buffers with a controlled reference circuit," in *Proc. ASIC Conf.*, Sep. 1997, pp. 311–315.

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