Low-Voltage Low Power Switchable Current Source LVDS Driver

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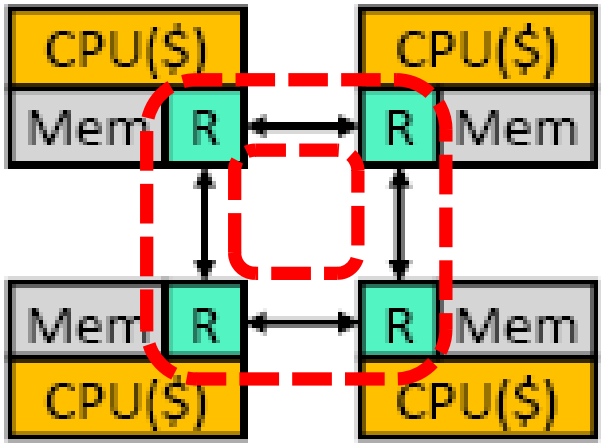
EECS 413 Final Project

LVDS

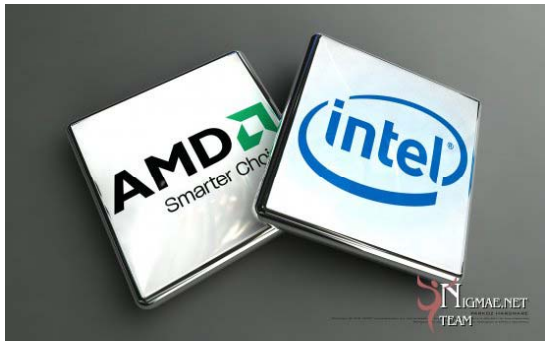
- Low Voltage Differential Switching
- Physical layer for I/O interface
- High-speed and Low Power



Slides developed in part by Profs. Falsafi, Hill, Hoe, Lipasti, Martin, Roth Shen, Smith, Sohi, and Vijaykumar of Carnegie Mellon University, Purdue University, University of Pennsylvania, and University of Wisconsin.

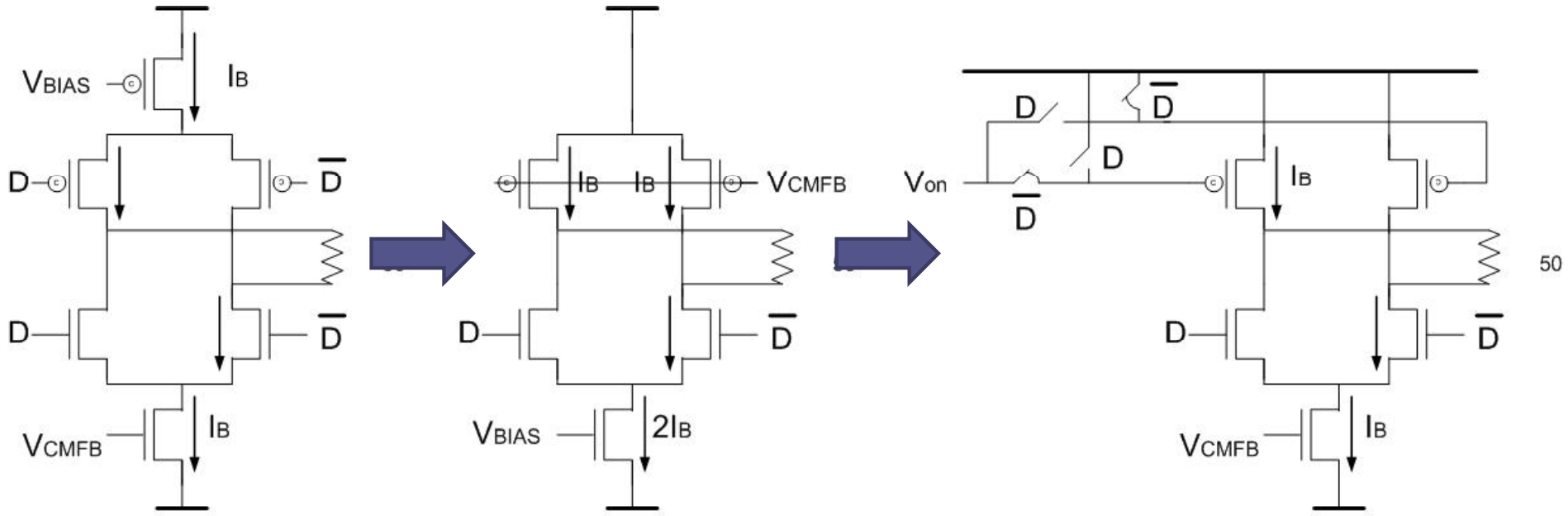
Design Specifications

- High speed I/O interface
  - PCI-Express (Intel)
  - HyperTransport (AMD/TI)
  - SERDES (IBM/Cisco)
- IEEE Standard 1596.3



Output Voltage Swing	±350mV
Data Rate	1Gb/s
Static Power Consumption	12.8 mW
Supply Voltage	1.8V

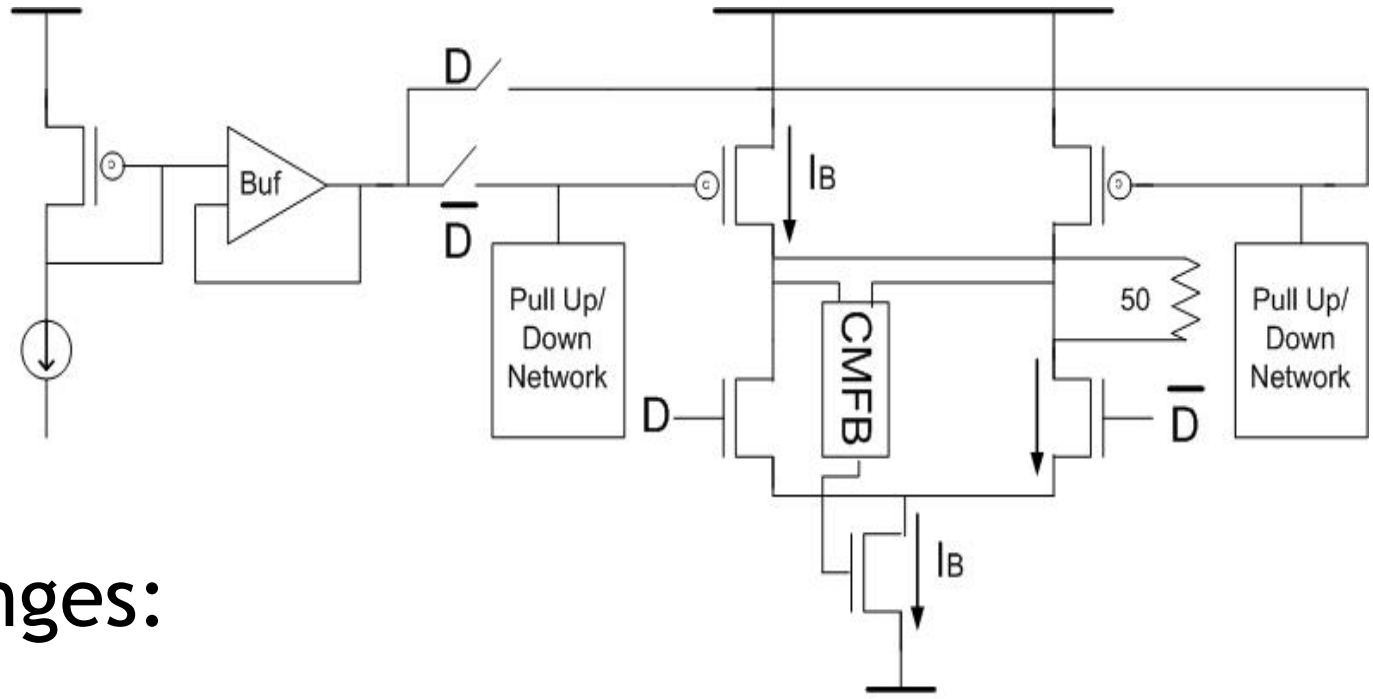
LVDS - Designs



Traditional LVDS DCS LVDS SCS LVDS

- LVDS requirement:
  - Output voltage swing range~ 250-400 mV
  - Output common-mode voltage~ 0.5 VDD

LVDS - Overview

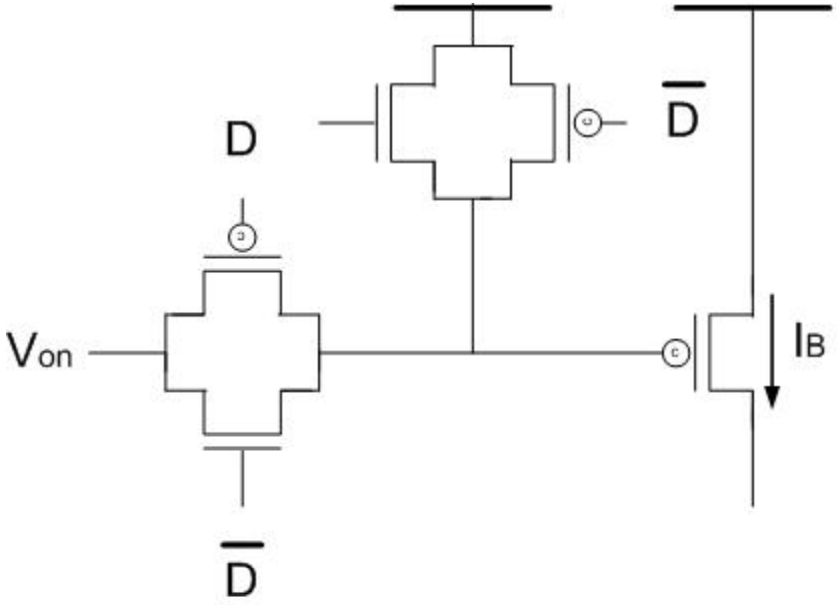


SCS LVDS

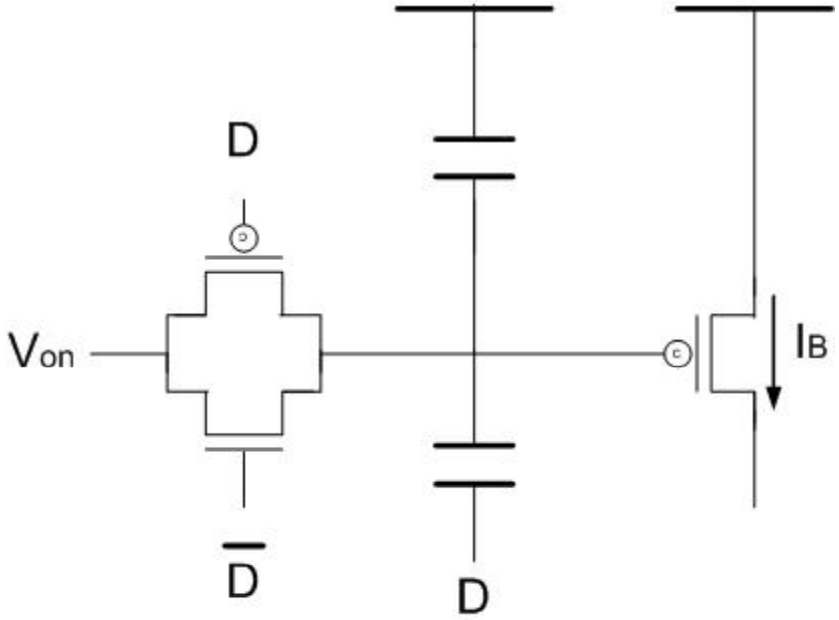
- Challenges:
  - Speed
  - Process Invariant

Pull Up/down Circuitry

- Two Implementation Styles

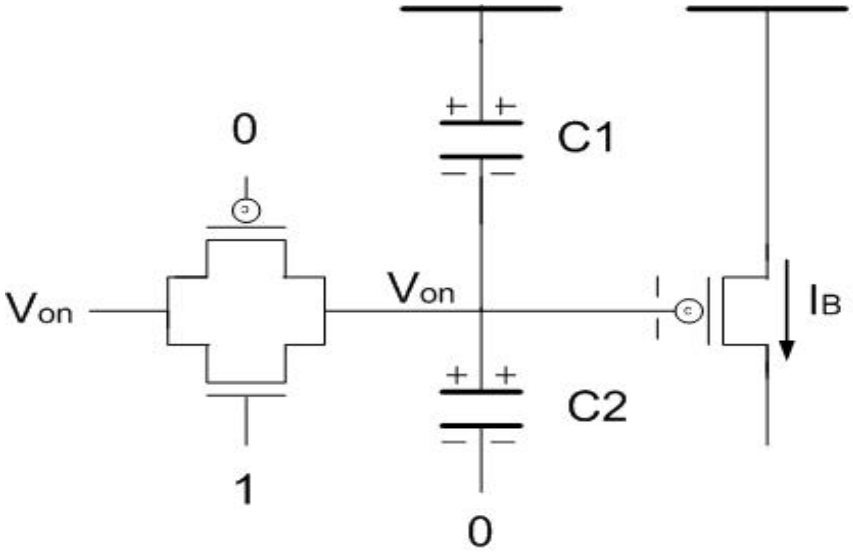


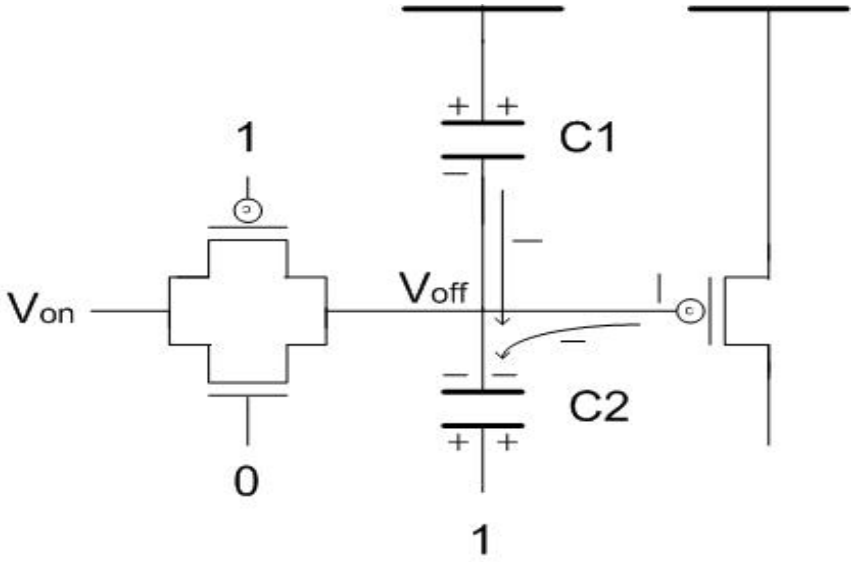
Transmission Scheme



Capacitive Voltage Divider Scheme

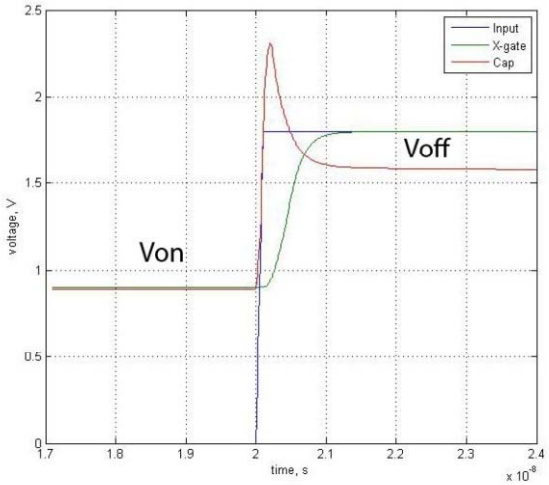
Pull Up/down Circuitry





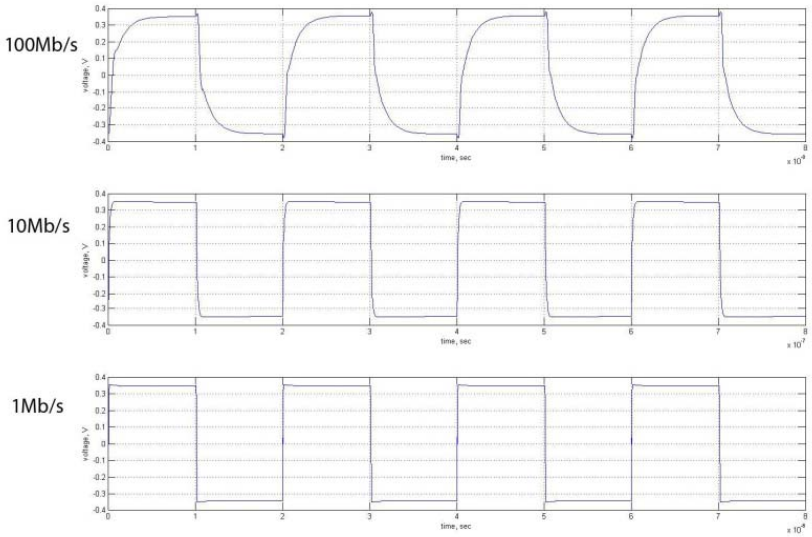
$$V_{off} - V_{on} = V_{DD} \cdot \left(\frac{C2}{C2 + C1} \right)$$

- Delay:
  - Transmission Scheme ~400ps
  - Capacitive Scheme ~20ps

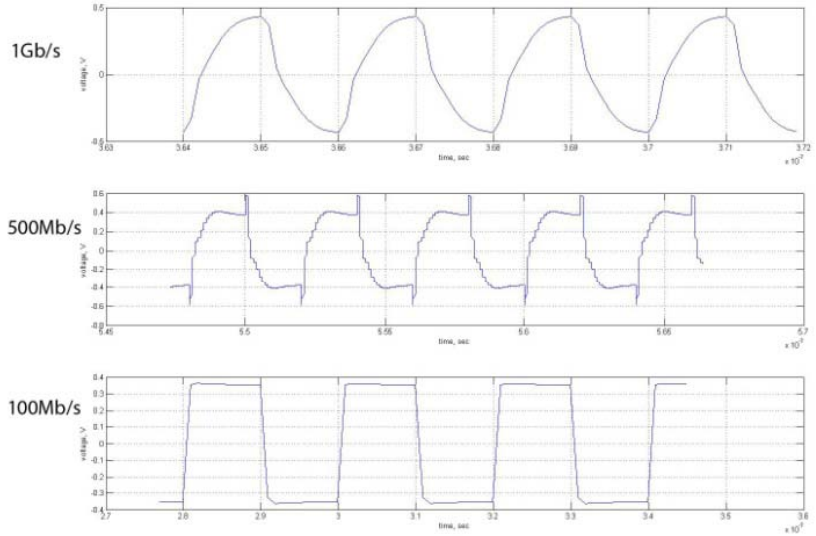


Performance

- Transmission Scheme : 100Mb/s
- Capacitive Scheme : 1Gb/s (10X Speedup)



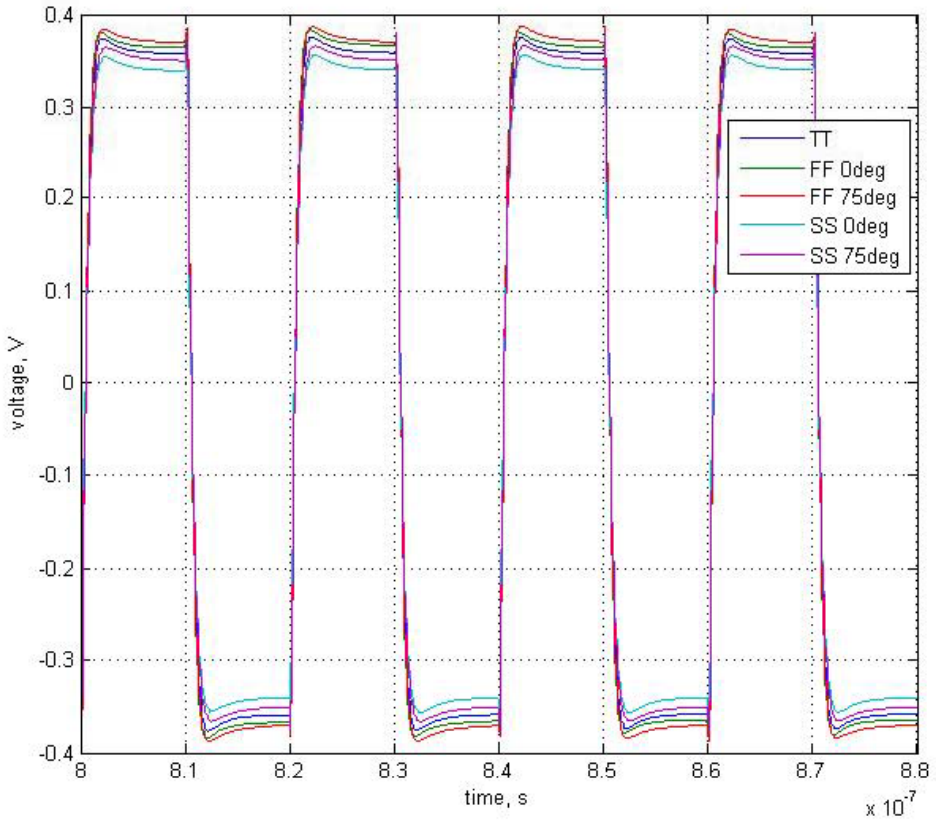
Transmission Scheme



Capacitive Scheme

Performance

- DM Transient over process and temperature



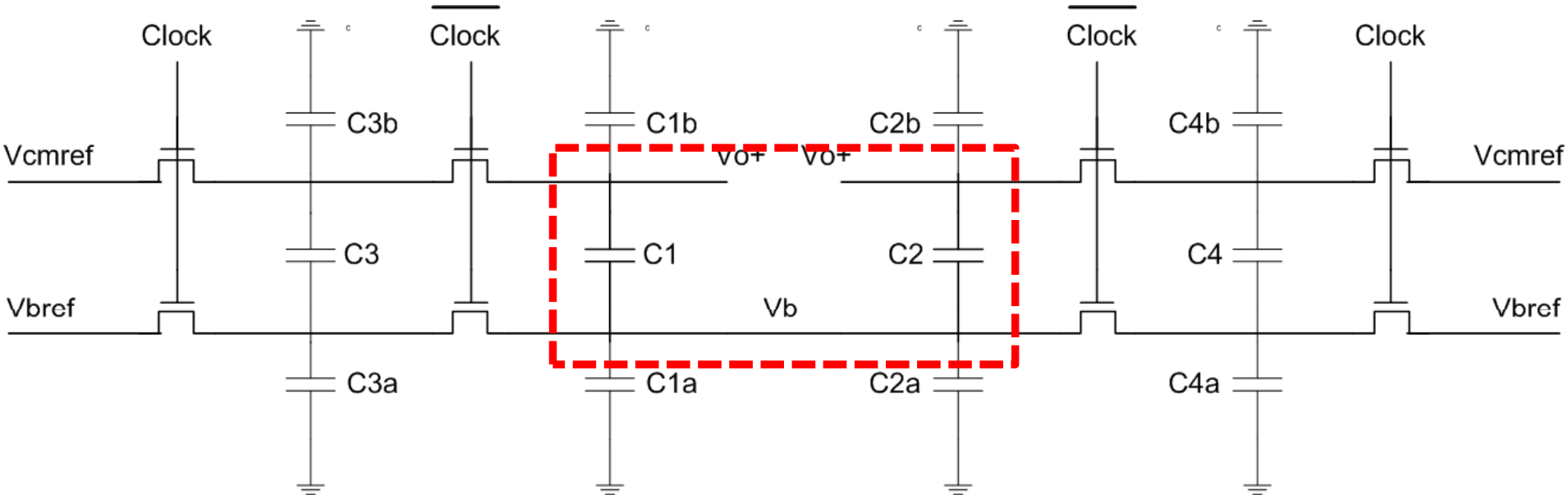
CMFB

- Purpose :
  - Maintain bias conditions
  - Reduce susceptibility to process and power supply variation

- Switched Capacitor CMFB
  - Low power
  - Not limited by differential input swings
  - Has little dependence on PVT

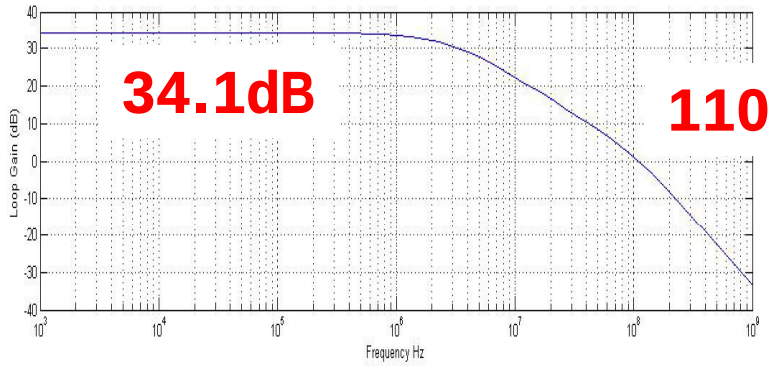
CMFB

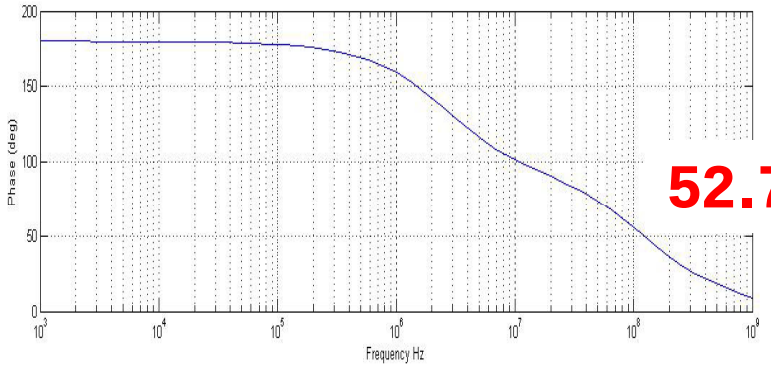
- Topology (SC-CMFB)

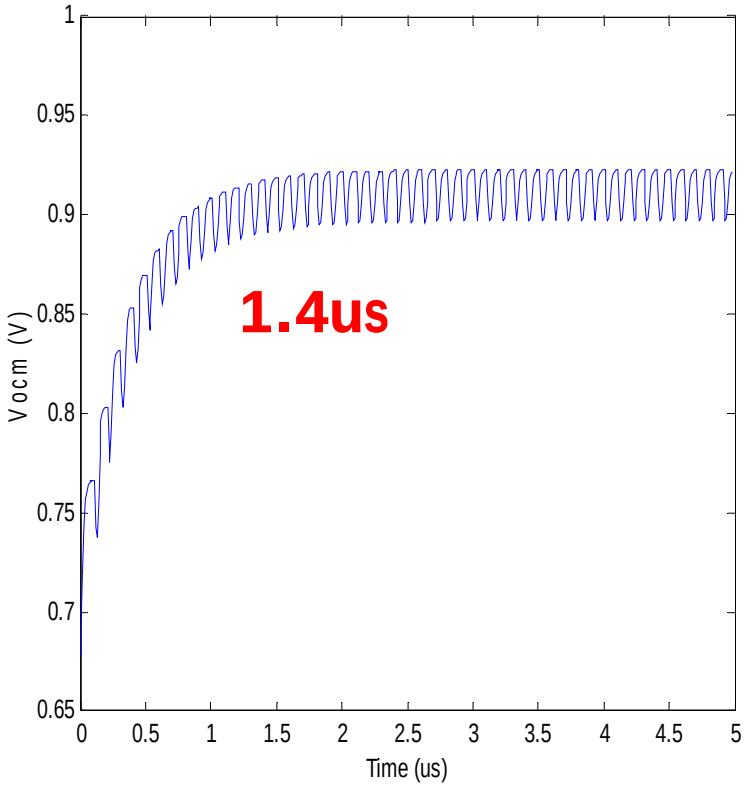


CMFB

- Results







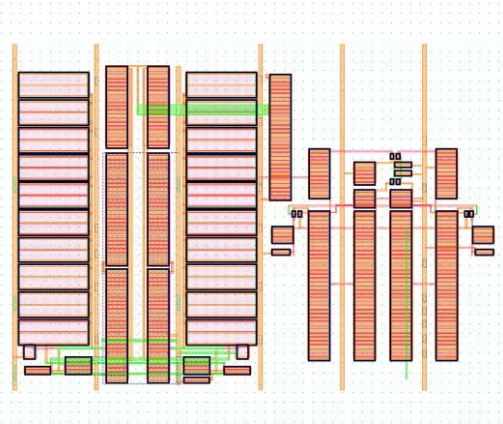
Conclusion

	SCS	Conventional [1]
Max Data Rate	1.2 Gb/s	1.2 Gb/s
Static Power Consumption	12.8 mW	43 mW
Supply Voltage	1.8 V	3.3 V
Output Voltage Swing	350 mV	412 mV
Technology	0.5 μm CMOS	0.35 μm CMOS

[1] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s per-Pin operation in 0.35um CMOS," IEEE J. Solid-State Circuits, vol. 36, no.4, pp.706-711, Apr. 2001.

Thank You

Q & A



Special thanks to Prof Wentzloff and Danial Enyaie