Low-Voltage Low-Power Switchable Current Sources (SCS) LVDS driver for 1 Gb/s Data Transmission

ChienHsun Lee, Evan Li

I. Introduction

Low power differential signaling (LVDS) is an IEEE standard for Gigabit/s serial data transmission and forms the physical layer for many modern ASIC I/O protocols such as PCI Express (Intel), Hyper-transport (AMD) and SERDES (IBM). As processing speed becomes increasingly limited by interconnection, high-speed low-power LVDS drivers are strongly desired.

II. Motivation

Conventional LVDS drivers cannot operate with low voltage supplies due to a lack of headroom. Our proposed design shown in Fig. 1 uses a 1.8V supply and is ideal for low-power applications. In addition, susceptibility to noise is significantly reduced with a differential switch design. However, such a topology requires common mode feedback (CMFB) to reject common mode (CM) gain. The proposed design also features a circuit technique that allows us to achieve a 1GHz DDR data rate at the expense of process and temperature (PVT) tolerance using a 0.5µm process. To minimize reflection, the transmission line is modeled as a 50Ω load impedance. This paper is organized as follows: Section III describes the design and performance of the switchable current source driver core, Section IV the input switch pull up and pull down networks and Section V the CMFB circuit. Finally, results are summarized in Section VI.

III. Switchable Current Source (SCS) LVDS Driver Core

Traditional LVDS design stacks four transistors in series. In our switchable current source LVDS design, we reduce the number of stack transistors while maintaining the same bias current. With the increased headroom, we were able to implement our design in low power environment to $1.8V_{DD}$. The basic operating principle of SCS LVDS uses alternating current sources to generate a required output swing range at a common-mode voltage of $V_{DD}/2$. The alternating current source is made possible by two PMOS turning on and off at different inputs. The output swing is controlled by the amount of current conducted. An approximated current of 7mA is required to generate an output swing of 350mV under a 50Ω load through a reference voltage applied to the PMOS. The reference voltage is generated through a current mirror of 0.1mA. The bottom NMOS is biased to sink 7mA.

Since a large current is conducted by the PMOS, both the size of the transistor and parasitic capacitance are huge. In order to operate at 1 Gb/sec, the rate of charging and discharging the parasitic capacitance at the gate of PMOS current source becomes a speed limiting factor. Slew rate is 600ps. DC CM characteristic is presented in Section V.

IV. Pull-up/down Network

In this section, we will compare two implementations for the pull-up/down network – a simple transmission gate scheme versus a passive pull up/down scheme shown in Fig 2. Transmission gates are sized to minimize latency. The passive circuit uses two capacitors as a capacitive voltage divider. When the switch is closed, the bottom capacitor C_{bottom} is being charged to V_{on}. When switch is open, charge distribution occurs, setting the gate voltage as shown in the following equation.

$$V_{gate} = V_{DD} \cdot \left(\frac{C_{top}}{C_{top} + C_{bottom}}\right)$$

In this design, the top capacitance C_{top} = 2pF, C_{bottom} = 4pF and gate voltage swing = 0.6V. The output voltage switches between V_{on} and off voltage V_{off}. The off voltage is designed to be 1.5V which effectively turns off the transistor minimizing leakage. The result shows that transmission gate scheme can only operate up to 100 Mb/s. The passive pull up/down circuit is capable of operating at up to 1 Gb/sec. Fig 3 shows the DM transient response for both schemes.

V. CMFB Circuit

The main drawback associated with a fully differential approach is the need for a CMFB circuit. Besides requiring extra area and power, the CMFB circuit diminishes driver performance by adding load impedance. The design uses a switched-capacitor CMFB circuit similar to that in [3]. From Fig. 4, we observe that CM output levels off and stabilizes at $V_{DD}/2$, the nominal CM output. Fig 5 shows a simplified model of the proposed topology. The circuit essentially operates in two phases. During the pre-charge phase, C1 and C2 are refreshed via C3 and C4. Therefore, their dc voltages are defined to be the difference between the reference bias voltage V_{bref} and reference CM output voltage V_{cmref}. During the evaluation phase, C1 and C2 averages the two outputs of the driver core, Vo+ and Vo-, and form an ac feedback path to the gate of the base transistor. A switched capacitor (SC-CMFB) topology is particularly suited for low-voltage low-power SCS type applications for three main reasons. First, it does not consume any extra power, other than dynamic power used by the pass transistors. Second, it is not limited by the differential input swing as opposed to CM voltage sensing methods using triode devices. Finally, the absence of active devices means that a SC-CMFB circuit has little or no PVT dependencies.

Assuming feed-forward CM gain A_{cm} is large and ignoring charge leakage, the steady state CM output voltage V_{ocm} and bias voltage V_b are defined by the following equation.

$$V_{ocm}[\infty] - V_b[\infty] = (V_{cmref} - V_{bref}) + \left(\frac{C_{p3}}{C_{p3}}\right) \cdot (V_B - V_{bref})$$

where V_B is the nominal bias voltage. Note that V_B does not necessarily equal V_{bref}. In order to minimize the effect of a mismatch between V_B and V_{bref}, the factor C_{p3}/C_3 must be scaled as small as possible. Furthermore, it can also been shown that the CM output settling time is determined by the C_3:C_1 ratio. Therefore, for C3 >> C1, the CMFB circuit reaches its steady state faster after start-up. Other capacitors are then sized to reflect the charge distribution during steady state. Scaling total capacitance increases CM unity-gain bandwidth (CM_{unity}) but adversely affects differential mode (DM) bandwidth (DM_{unity}). For $C_3 = C_4$ = 1.5pF, $C_{3a} = C_{4a}$ = 75fF, $C_{3b} = C_{4b}$ = 240fF, $C_1 = C_2$ = 75fF, $C_{1a} = C_{2a}$ = 4fF and $C_{1b} = C_{2b}$ = 12fF, CM loop gain = 34.11dB, unity-gain frequency = 110MHz, phase margin = 52.7deg, and dc settling time = 0.8µs. Fig 6 shows the open loop ac response when data is stable (0V/1.8V). CM input is attenuated when data is meta-stable (0.9V). The CMFB circuit is clocked at 10MHz (< CM_{unity}).

VI. Summary

Fig 7 shows the layout of the proposed LVDS driver design. The LVDS driver employs switchable current sources to create extra headroom which allows us to drop V_{DD} to 1.8V. This could not have been possible in conventional LVDS drivers. As a result of V_{DD} scaling, power consumption is significantly reduced for a given output swing. We were able to achieve 1Gb/s data rate with the addition of a capacitive voltage divider. A SC-CMFB circuit is an efficient way of providing common feedback with minimal power consumption without excessive loading. Simulation results are summarized in Fig 8.

References

[1] J. Chen, J. Martinez, M. Nix, "Low-Voltage Low-Power LVDS Drivers," IEEE J. Solid-State Circuits vol. 40 no.2, Feb., 2005.

[2] A. Boni, A. Pierazzi, D. Vecchi, "LVDS I/O Interface for Gb/s-per-pin Operation in 0.35um CMOS," IEEE J. Solid-State Circuits vol. 36 no.4, Apr., 2001

[3] O. Choksi, L. Carley, "Analysis of Switched-Capacitor Common-Mode Feedback Circuit," IEEE Trans. Circuits and Systems II vol. 50 no.12, Dec., 2003

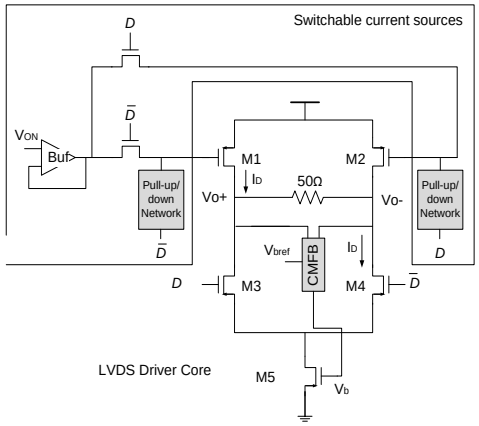
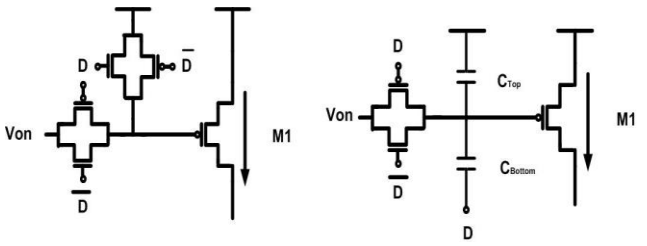


Figure 1: LVDS Driver schematic



Transmission gate scheme Passive scheme

Figure 2: Pull up/down networks : topology

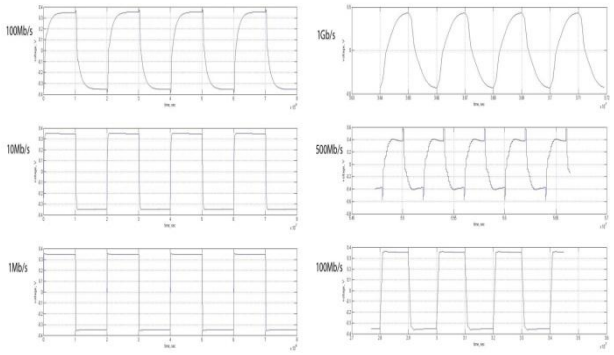


Figure 3: Transmission gate and passive scheme : DM transient response

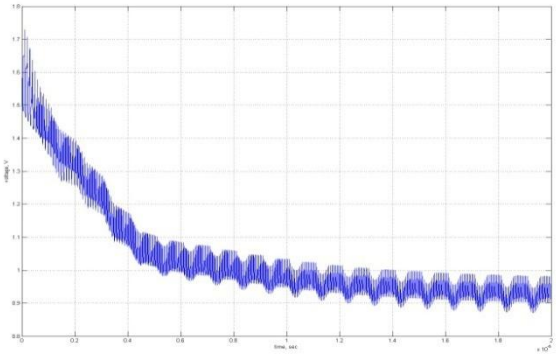


Figure 4: CM output Vocm: Transient response

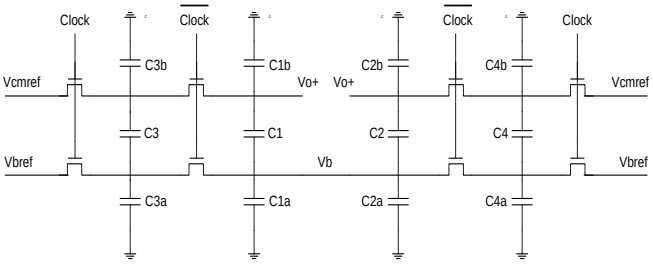


Figure 5: CMFB circuit : topology

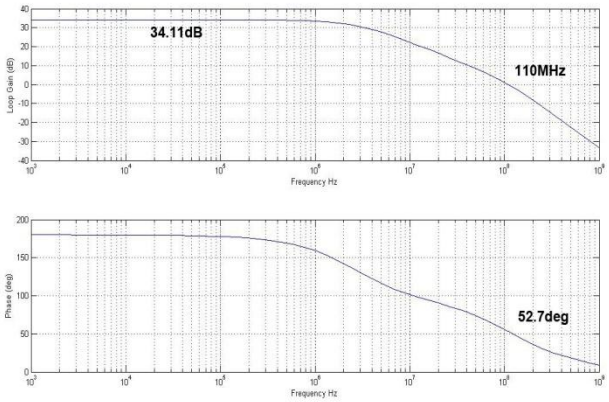


Figure 6: CMFB circuit : Open Loop AC response

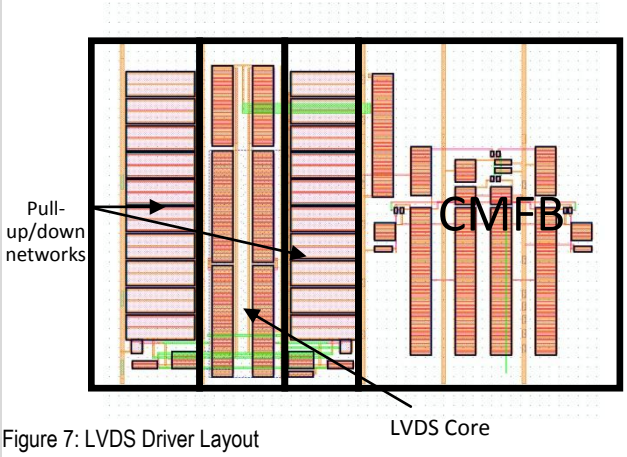


Figure 7: LVDS Driver Layout

Specification	Value	Units
VDD	1.8	V
Clock rate	500	MHz
Power	12.6	mW
DM 3dB Bandwidth	200	MHz
CM 0dB Bandwidth	110	MHz
CM Gain	34.2	dB
Phase Margin	52.7	deg

Figure 8: Table summarizing your results.