# EECS 470
# Power and Architecture

**Many slides taken from Prof. David Brooks, Harvard University and modified by Mark Brehob . A couple of slides are also taken from Prof. Wenisch. Any errors are almost certainly Mark's.**

**Thanks to both!**

# Outline



- **Why is power a problem?**
- **What uses power in a chip?**
- **Relationship between power and performance.**
- **How can we reduce power?**

# Why is power a problem in a µP?

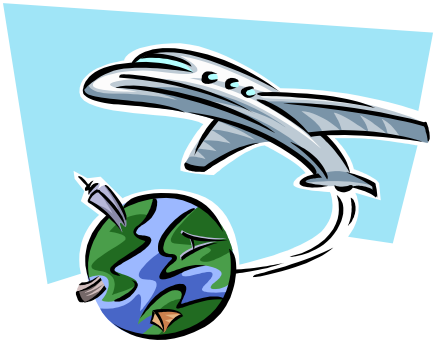


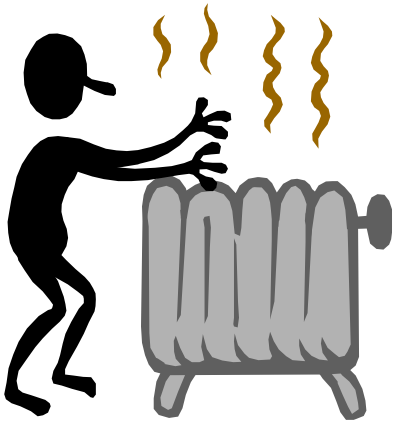
- Power used by the µP, vs. system power
- Dissipating Heat
  - Melting (very bad)
  - Packaging (to cool → $)
  - Heat leads to poorer performance.
- Providing Energy
  - Battery
  - Cost of electricity

# Why worry about power dissipation?



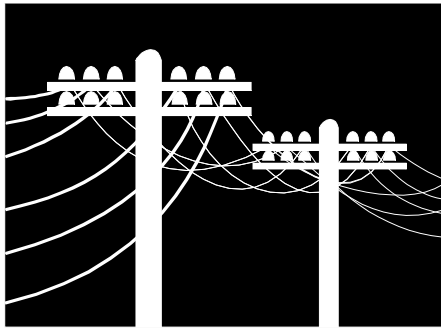
Battery life



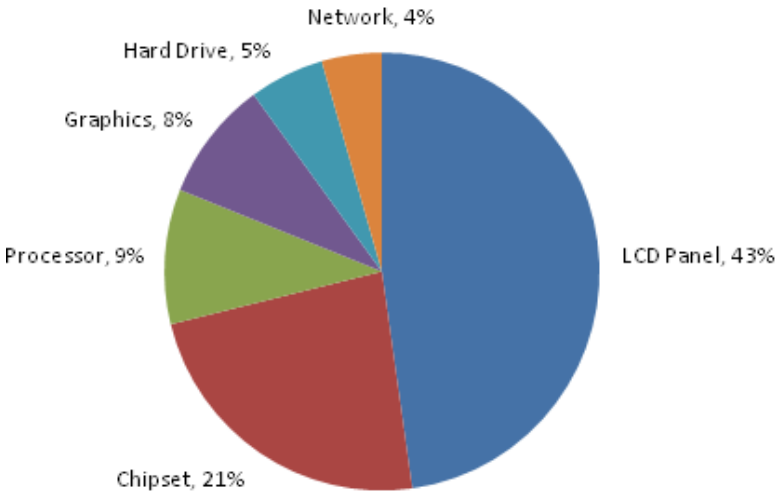


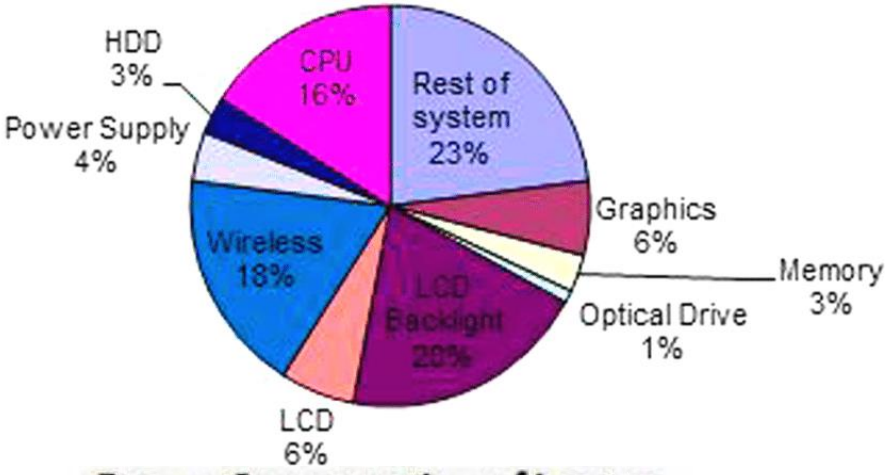
Thermal issues: affect cooling, packaging, reliability, timing

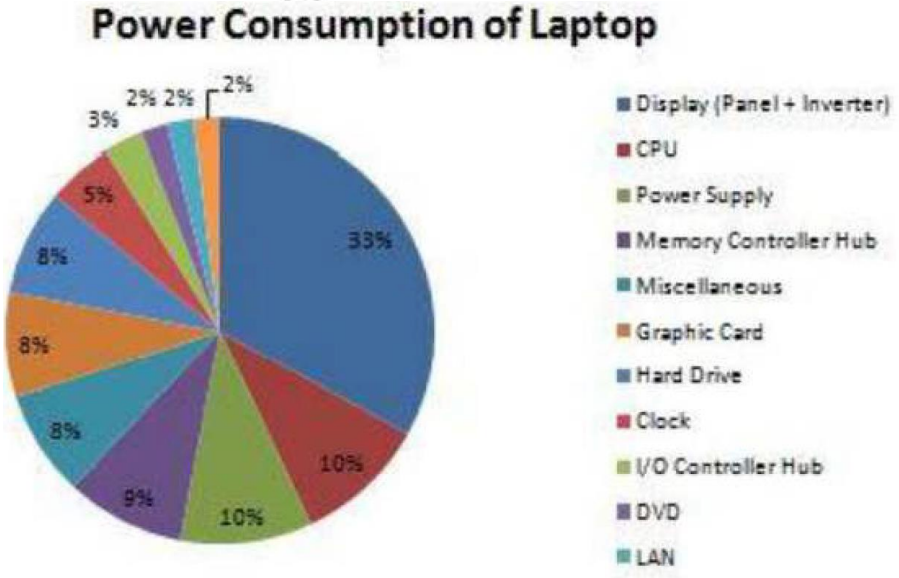
Environment



# Where does the juice go in laptops?

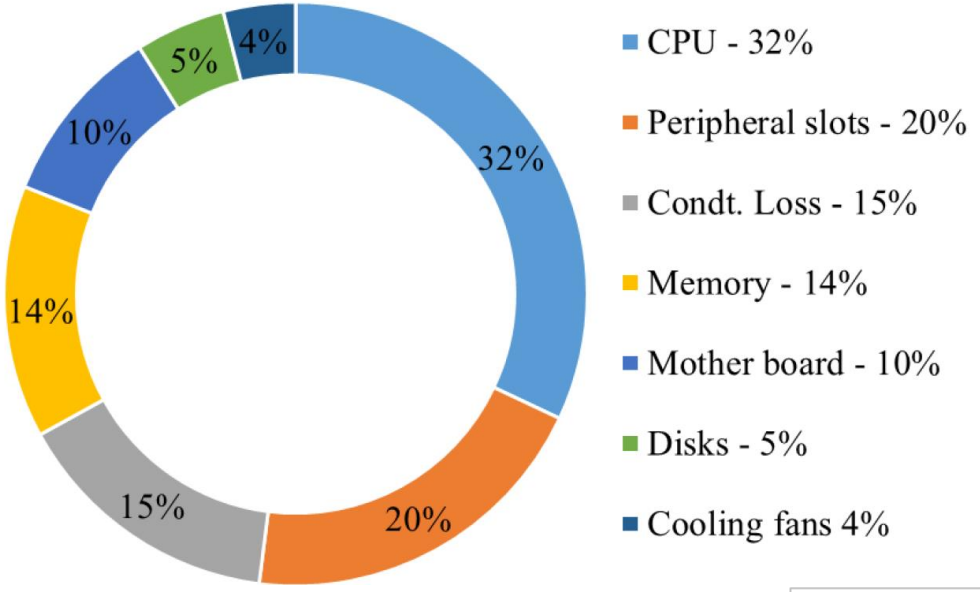


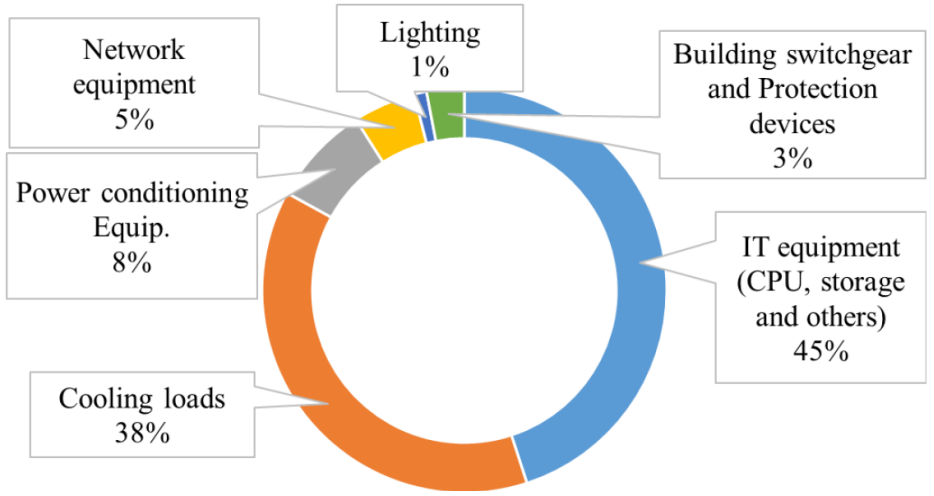




- **Left, Microsoft, 2009.**
- **Top Right, Samavat, 2011**
- **Bottom Right, Kumar, Kumar, Taruna 2020**

# Servers and data centers?

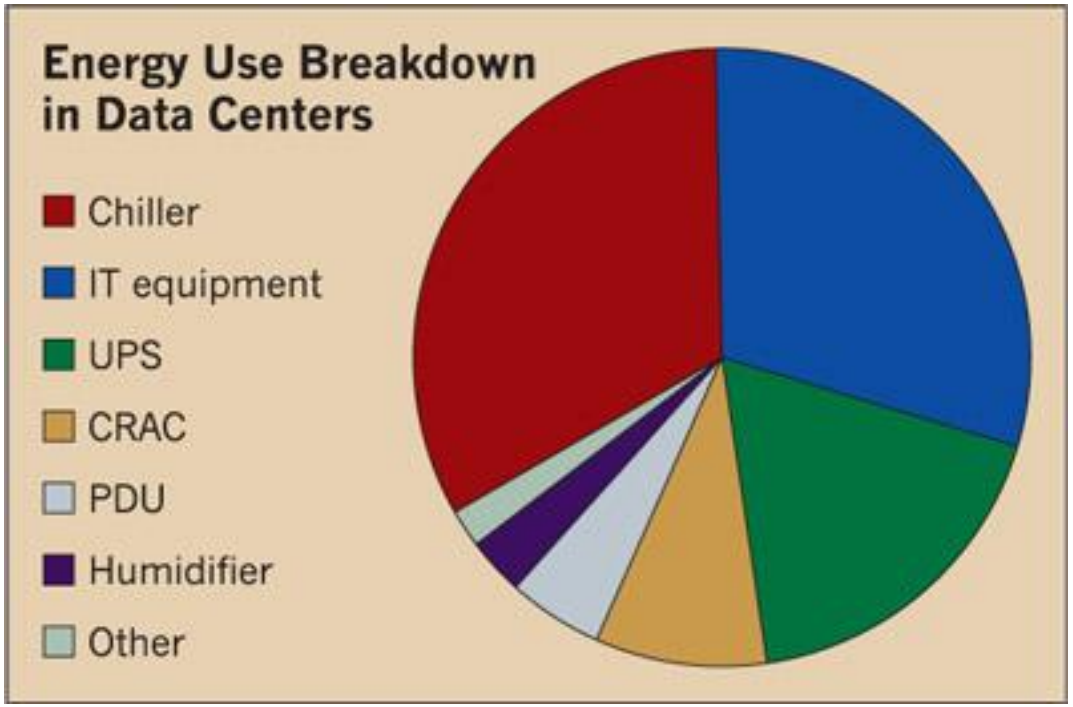



*Need whole-system approaches to save energy*

K.M.U. Ahmed et al.: A Review of Data Centers Energy Consumption And Reliability Modeling

# More data center

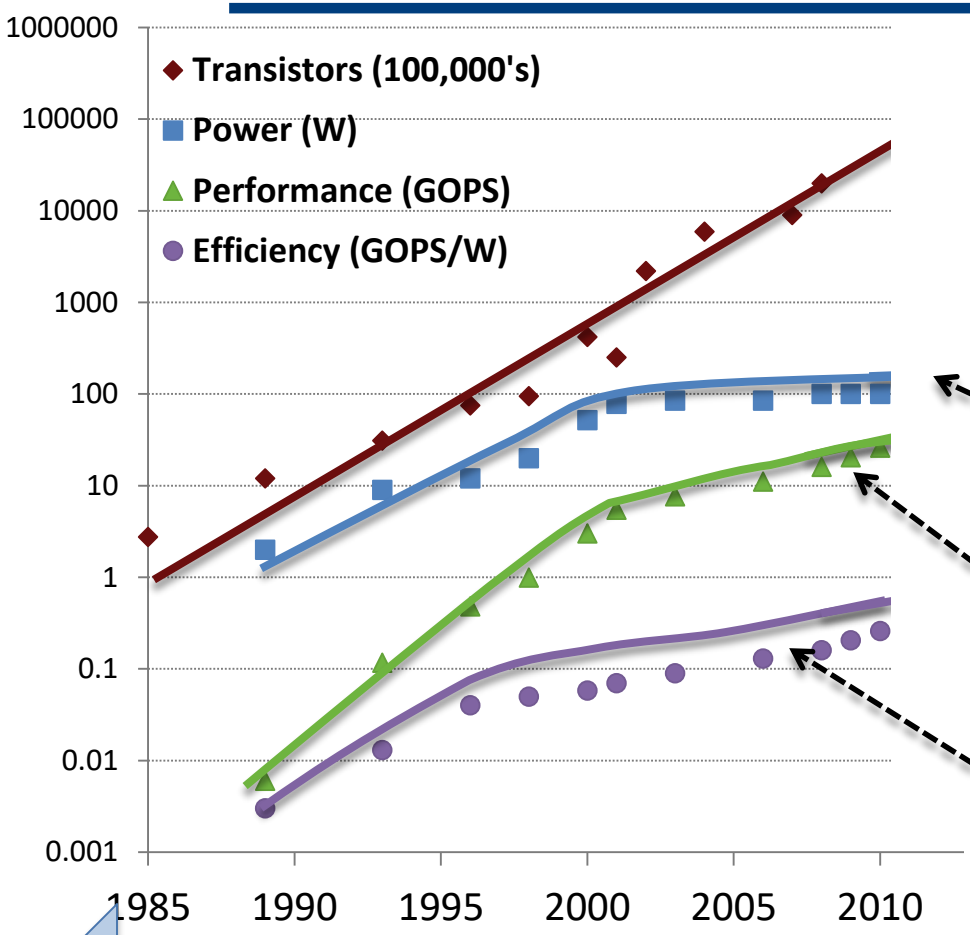


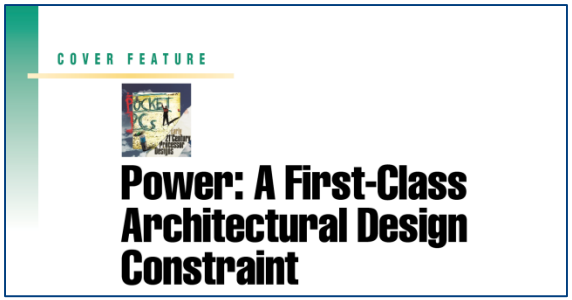

*Data Centers are about 1.5% of global electricity use as of 2023*

https://www.scientificamerican.com/article/the-ai-boom-could-use-a-shocking-amount-of-electricity

Power usage effectiveness (PUE)
A PUE of 2.0 means that for every 2W of power supplied to the data center, only 1W is consumed by computing equipment.
Values of around 2.9 are pretty common

# A Paradigm Shift In Computing




*IEEE Computer—April 2001*
*T. Mudge*

Limits on heat extraction

Stagnates performance growth

Limits on energy-efficiency of operations

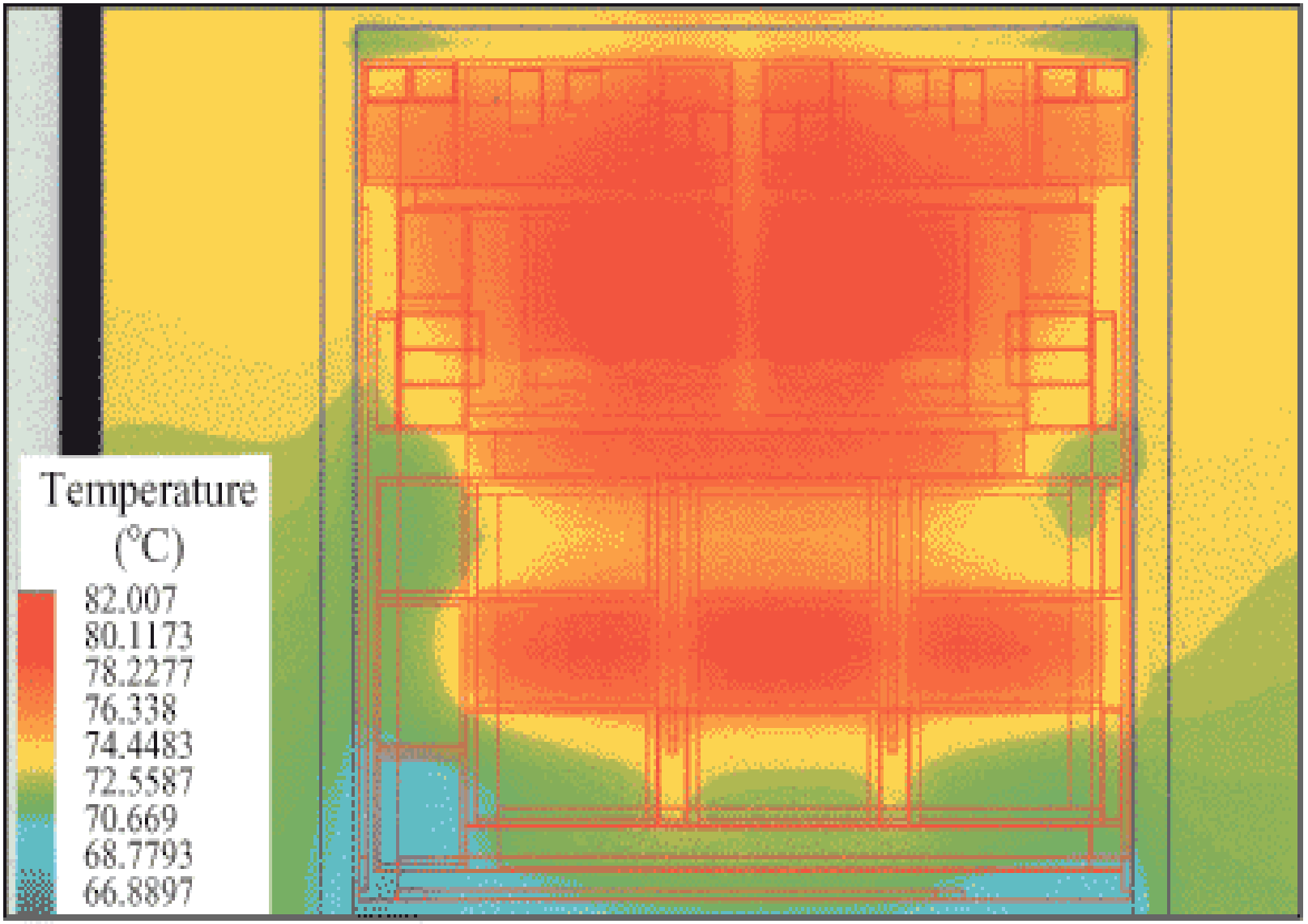
Era of High Performance Computing

*c. 2000*

Era of Energy-Efficient Computing

# Spot Heat Issues in Microprocessors

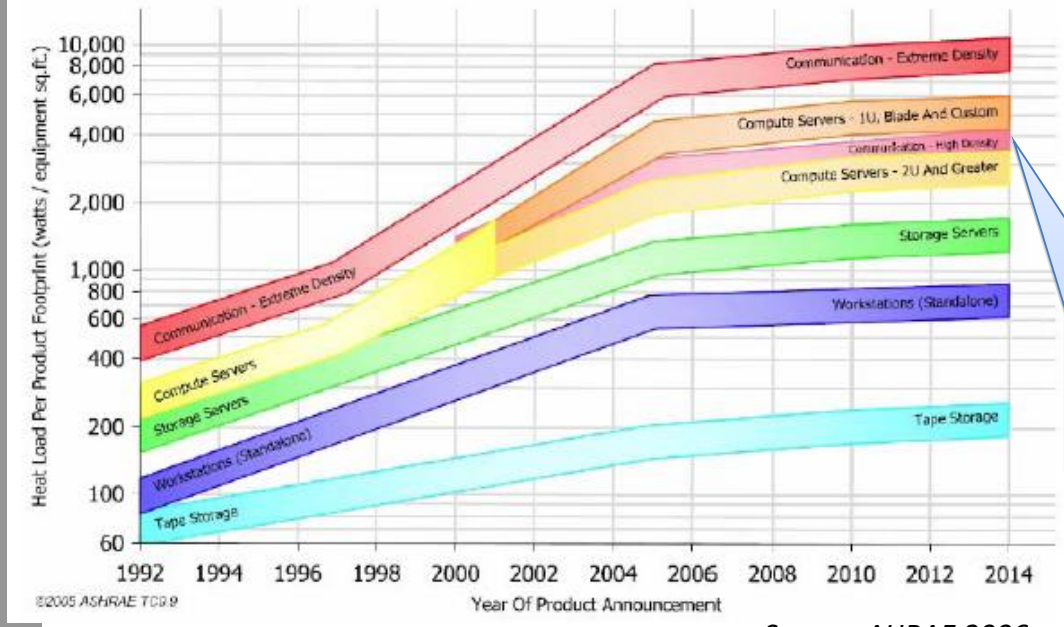
Why is power a problem?



# Why is cooling so costly? (1)

## Server density increasing

- **Integration, disaggregation reduce hardware costs**
- **Need for high-BW interconnect**
- **Data center floor space costs up to $15,000 /m$^2$**




Heat flux up to
500W per ft$^2$ floor space;
Racks draw 4 to 20kW each

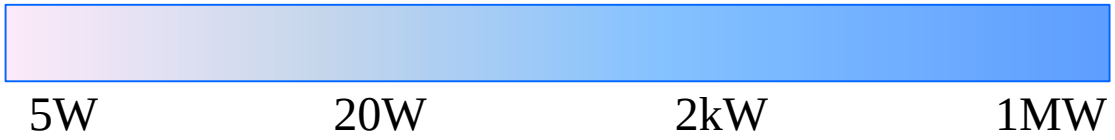
*Source: AHRAE 2006*

# Why is cooling so costly? (2)

**Heat density drives cooling cost**

**Cooling power grows super-linearly with thermal load**


Heat Generated




Power to Remove

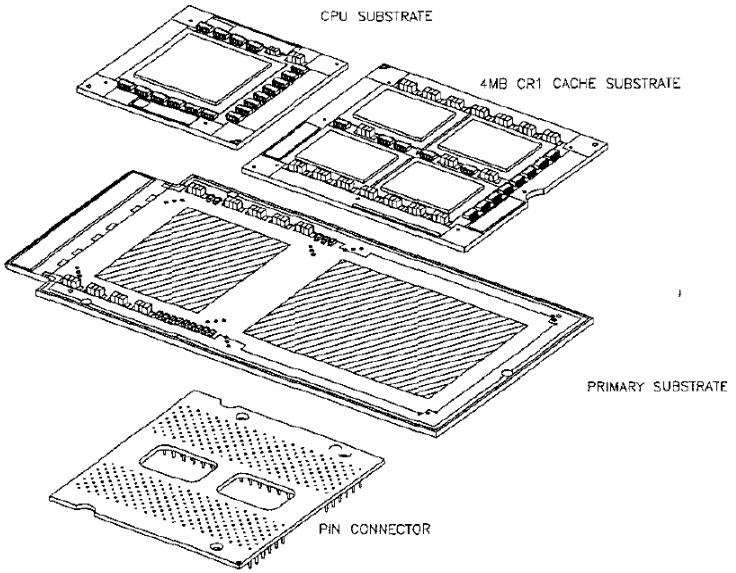
*Source: C. Patel, HP Labs*

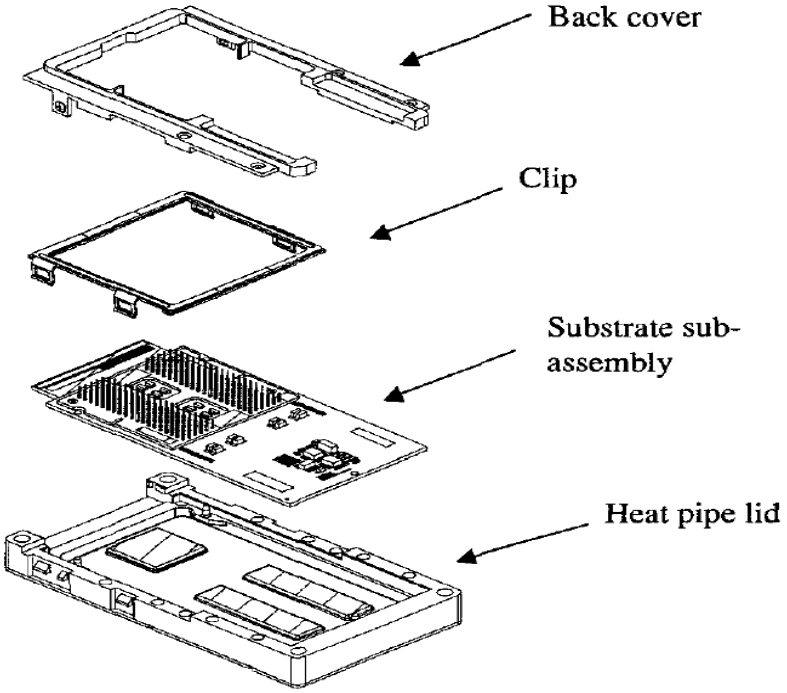
*Servers' 3-year power & cooling costs nearing their purchase price*

# Intel Itanium packaging



## Complex and expensive (note heatpipe)



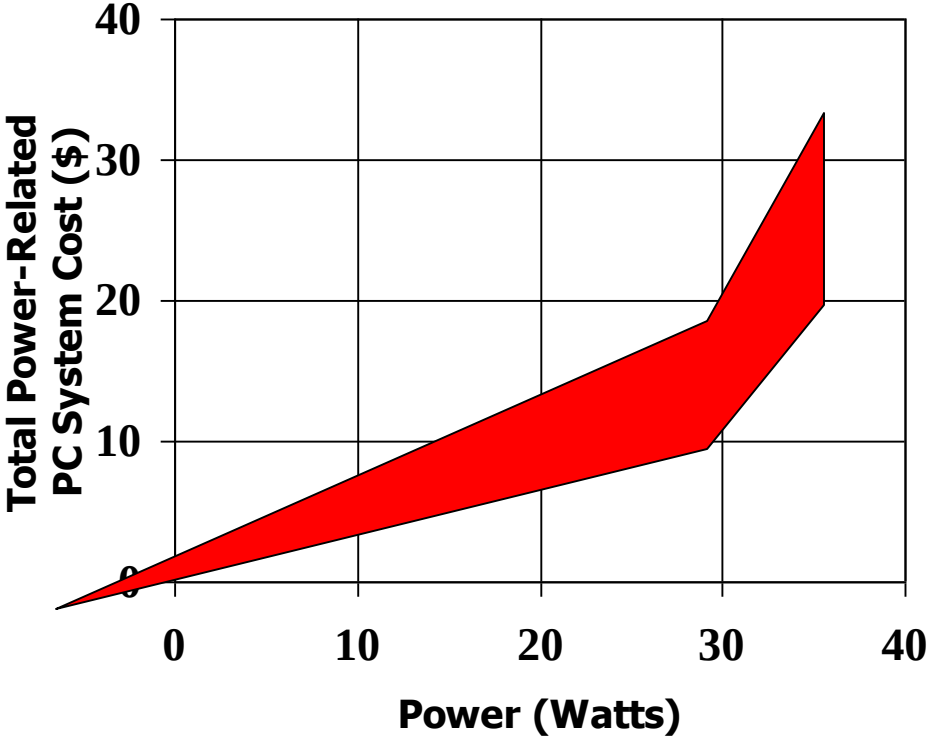




Source: H. Xie et al. “Packaging the Itanium Microprocessor” Electronic Components and Technology Conference 2002

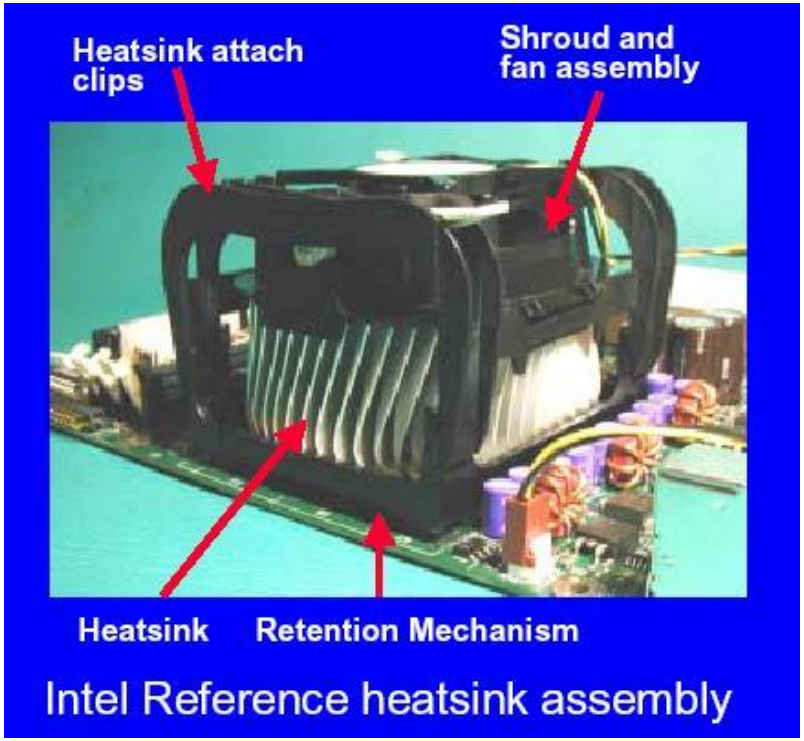
# P4 packaging



- **Simpler, but still…**




From Tiwari, et al., DAC98




Source: Intel web site

# Power-Aware Computing Applications

# Environment



- **Environment Protection Agency (EPA): computers consume 10% of commercial electricity consumption**
  - **This incl. peripherals, possibly also manufacturing**
  - **A DOE report suggested this percentage is much lower (3.0-3.5%)**
  - **No consensus, but it's still a lot**
  - **Total cost of electricity for *gaming computers* estimated at *$10 Billion/year*.**
    - **http://newscenter.lbl.gov/2015/08/31/gaming-computers-offer-huge-untapped-energy-savings-potential/**
- **Data center growth was cited as a contribution to the 2000/2001 California Energy Crisis**
- **Equivalent power (with only 30% efficiency) for AC**
- **Lap burn**
- **Fan noise**

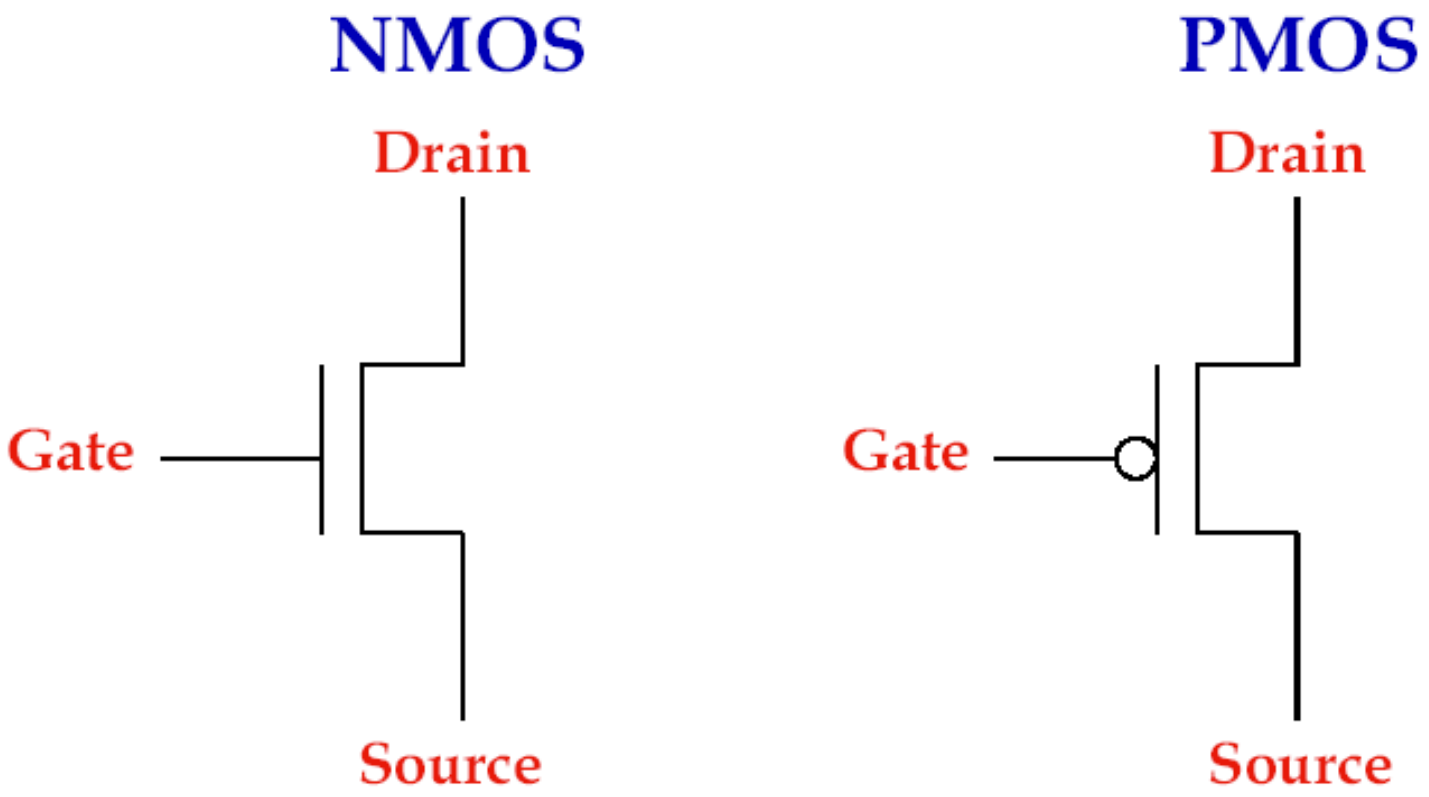
# Power-Aware Needed across all computing platforms



- Mobile/portable (cell phones, laptops, PDA)
  - Battery life is critical
- Desktops/Set-Top (PCs and game machines)
  - Packaging cost is critical
- Servers (Mainframes and compute-farms)
  - Packaging limits
  - Volumetric (performance density)

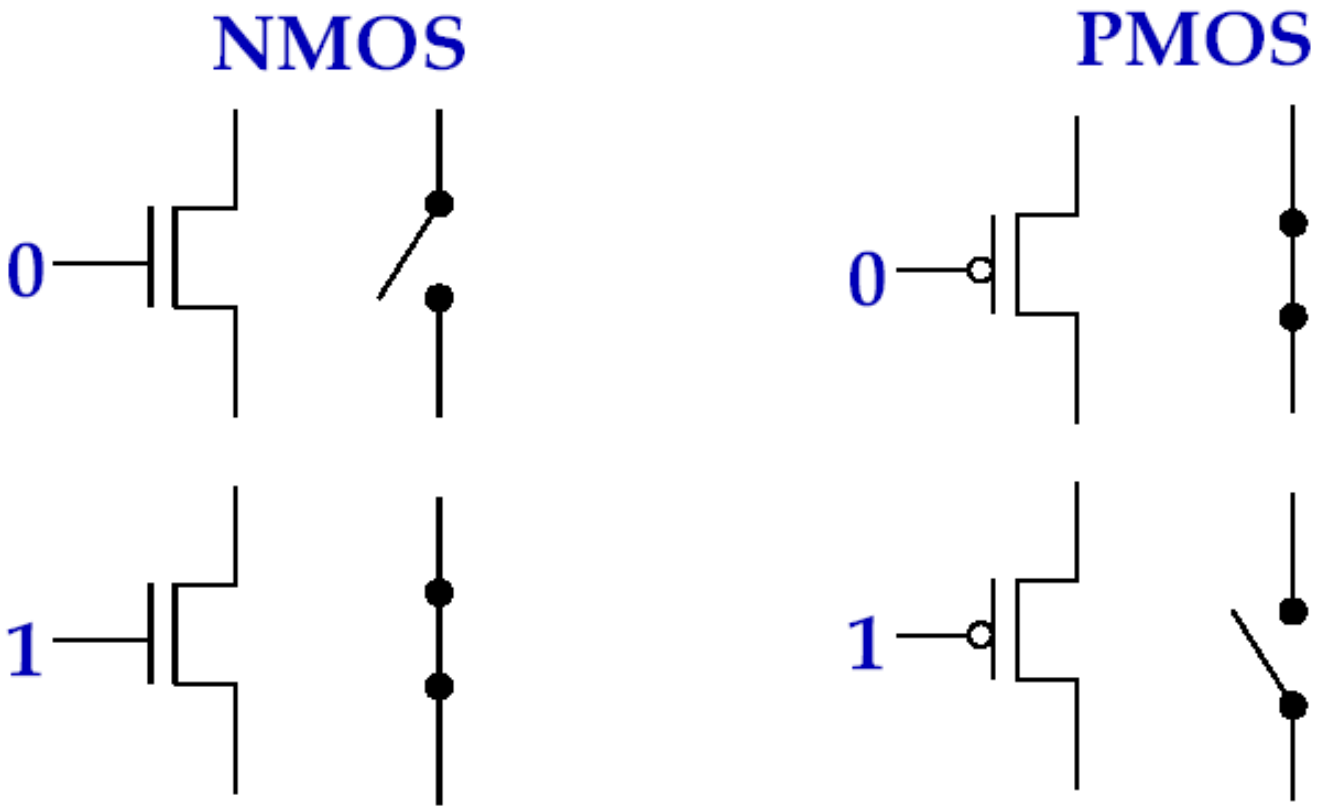
# How CMOS Transistors Work





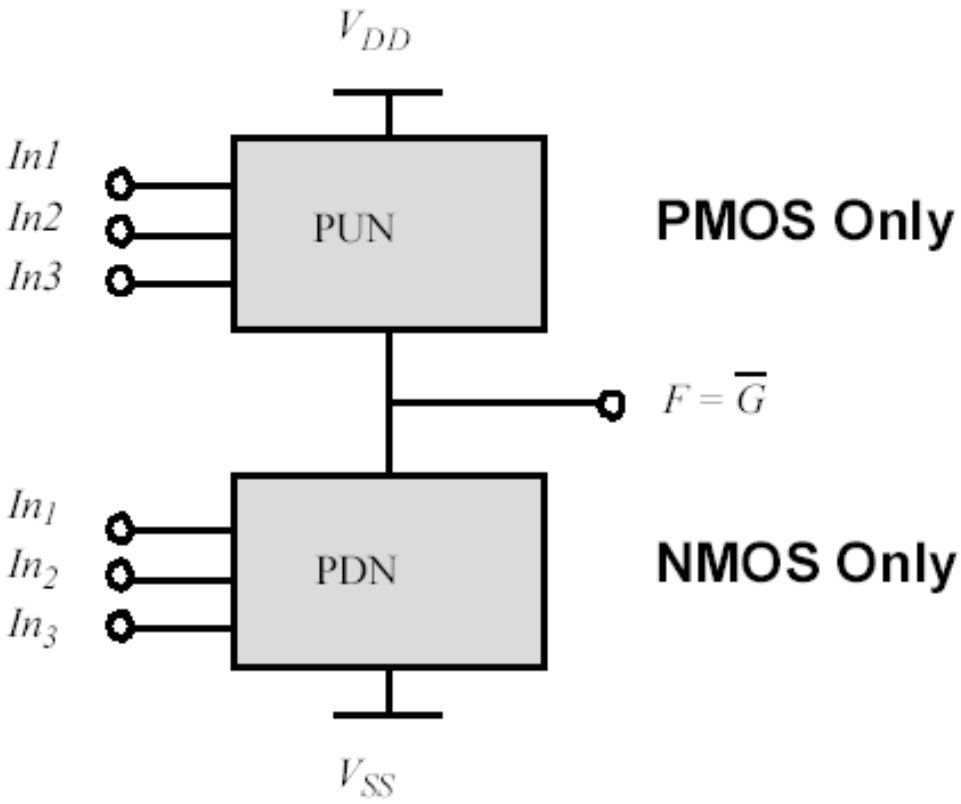
# MOS Transistors are Switches

What uses power in a chip?



# Static CMOS

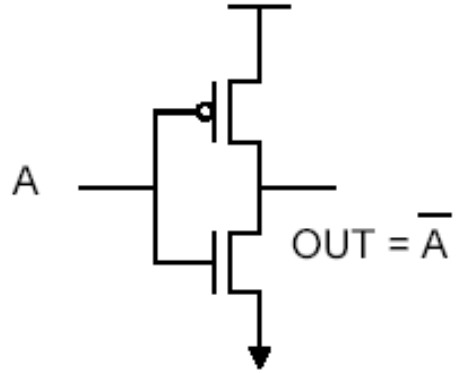
What uses power in a chip?

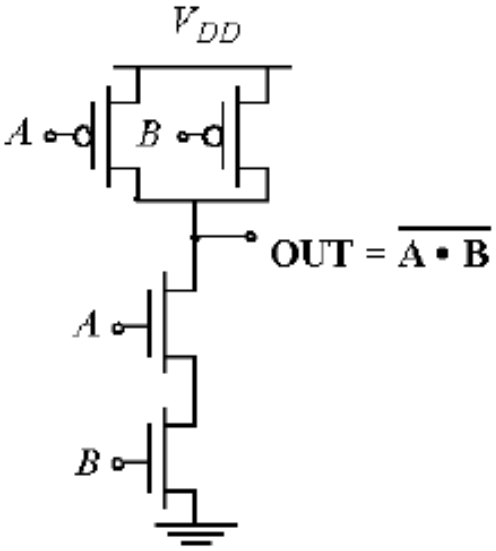


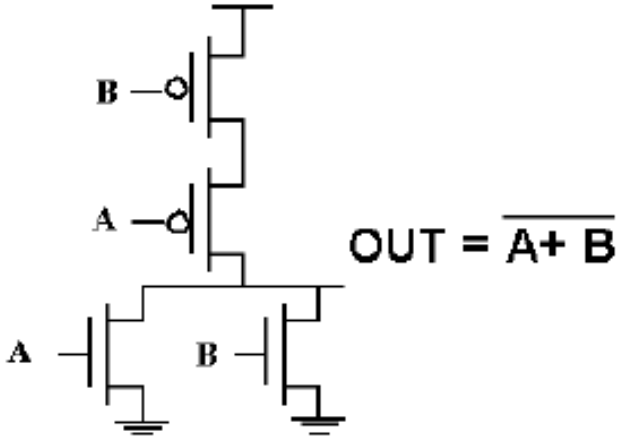

PUN and PDN are Dual Networks

# Basic Logic Gates

What uses power in a chip?



# CMOS Water Analogy



**Electron: water molecule**

**Charge: weight of water**

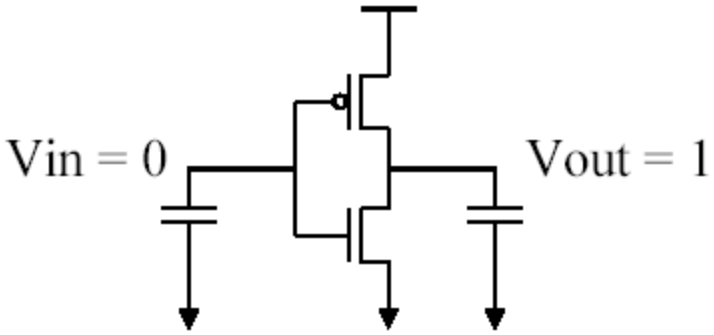
**Voltage: height**

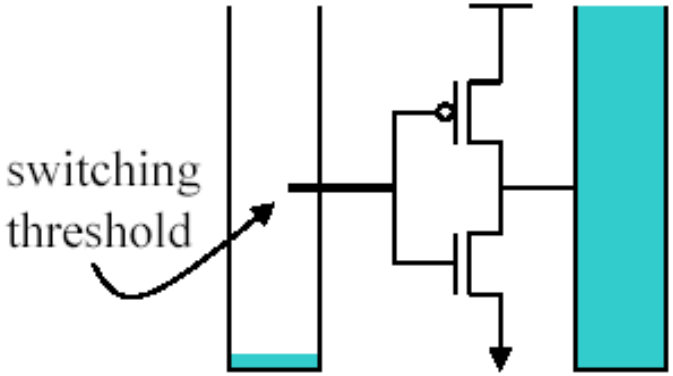
**Current: flow rate**

**Capacitance: container cross-section**

**(Think of power-plants that store energy in water towers)**

# Liquid Inverter




- Capacitance at input
  - Gates of NMOS, PMOS
  - Metal interconnect
- Capacitance at output
  - Fanout (# connections) to other gates
  - Metal Interconnect

NMOS conducts when water level is above switching threshold

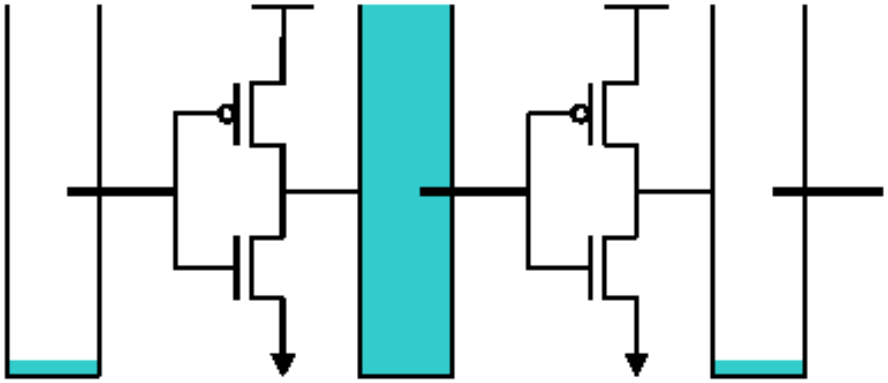
PMOS conducts below

No conduction after container full

Slide courtesy D. Brooks, Harvard

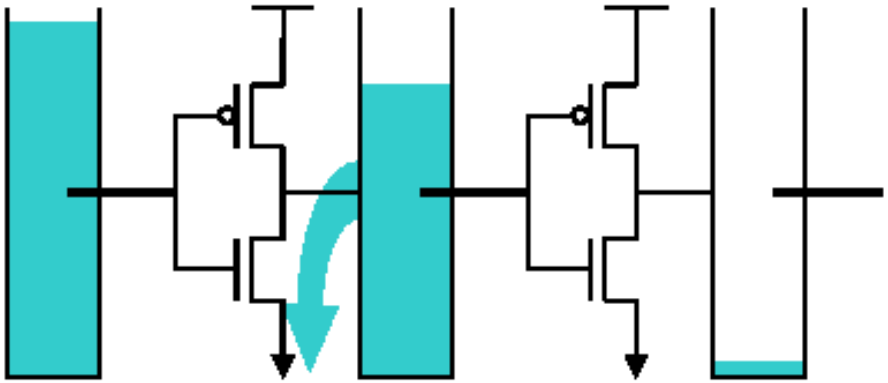
# Inverter Signal Propagation (1)

t < 0
Vin = 0



Vout = 0

t = 0
Vin = 1

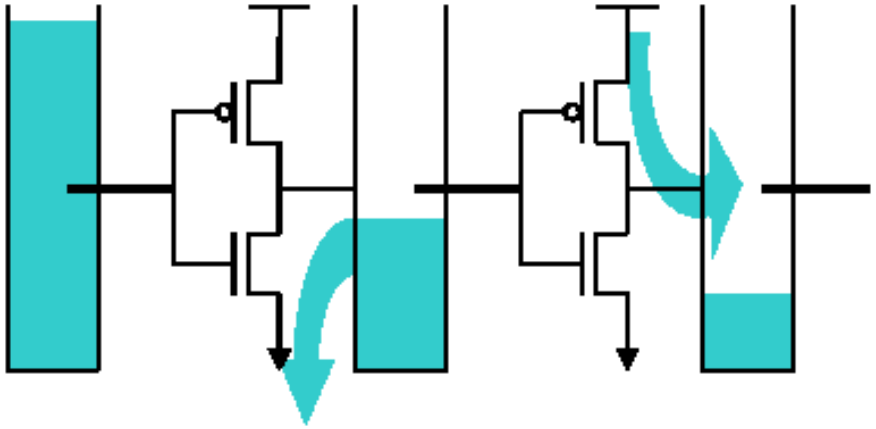


Vout = 0

Slide courtesy D. Brooks, Harvard

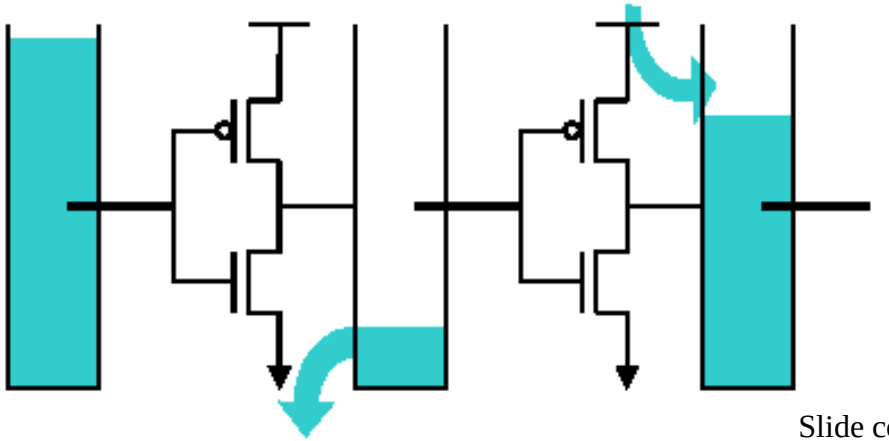
# Inverter Signal Propagation (2)

t = 1
Vin = 0



Vout = 0

t = 2
Vin = 1



Vout = 1

Slide courtesy D. Brooks, Harvard

# Delay and Power Observations



- **Load capacitance increases delay**
  - **High fanout (gates attached to output)**
  - **Interconnection**
- **Higher current can increase speed**
  - **Increasing transistor width raises currents but also raises capacitance**
- **Energy per switching event independent of current**
  - **Depends on amount of charge moved, not rate**

# Power: The Basics

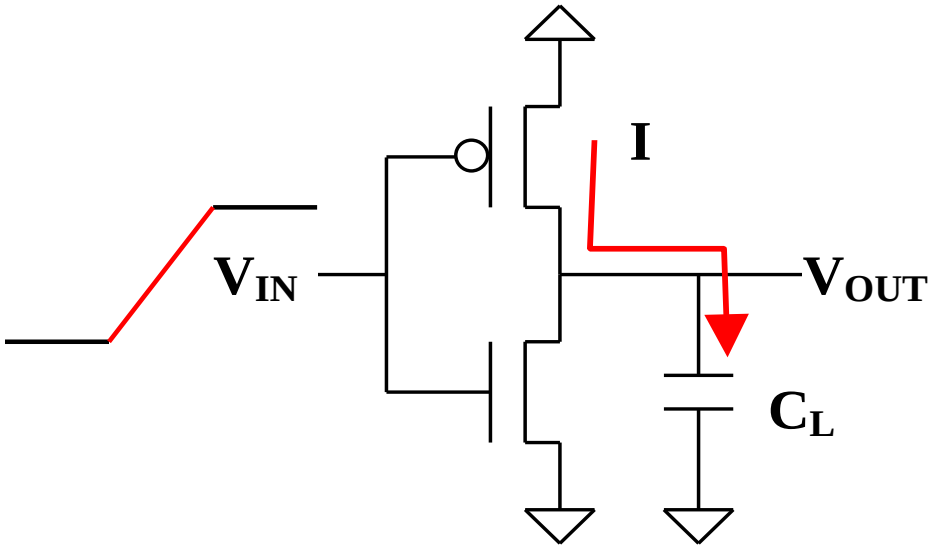
What uses power in a chip?

- Dynamic power vs. Static power
  - Dynamic: “switching” power
  - Static: “leakage” power
  - Dynamic power dominates, but static power increasing in importance

- Static power: steady, per-cycle energy cost
- Dynamic power: capacitive and short-circuit
- Capacitive power: charging/discharging at transitions from 0→1 and 1→0
- Short-circuit power: power due to brief short-circuit current during transitions.

# Dynamic (Capacitive) Power Dissipation

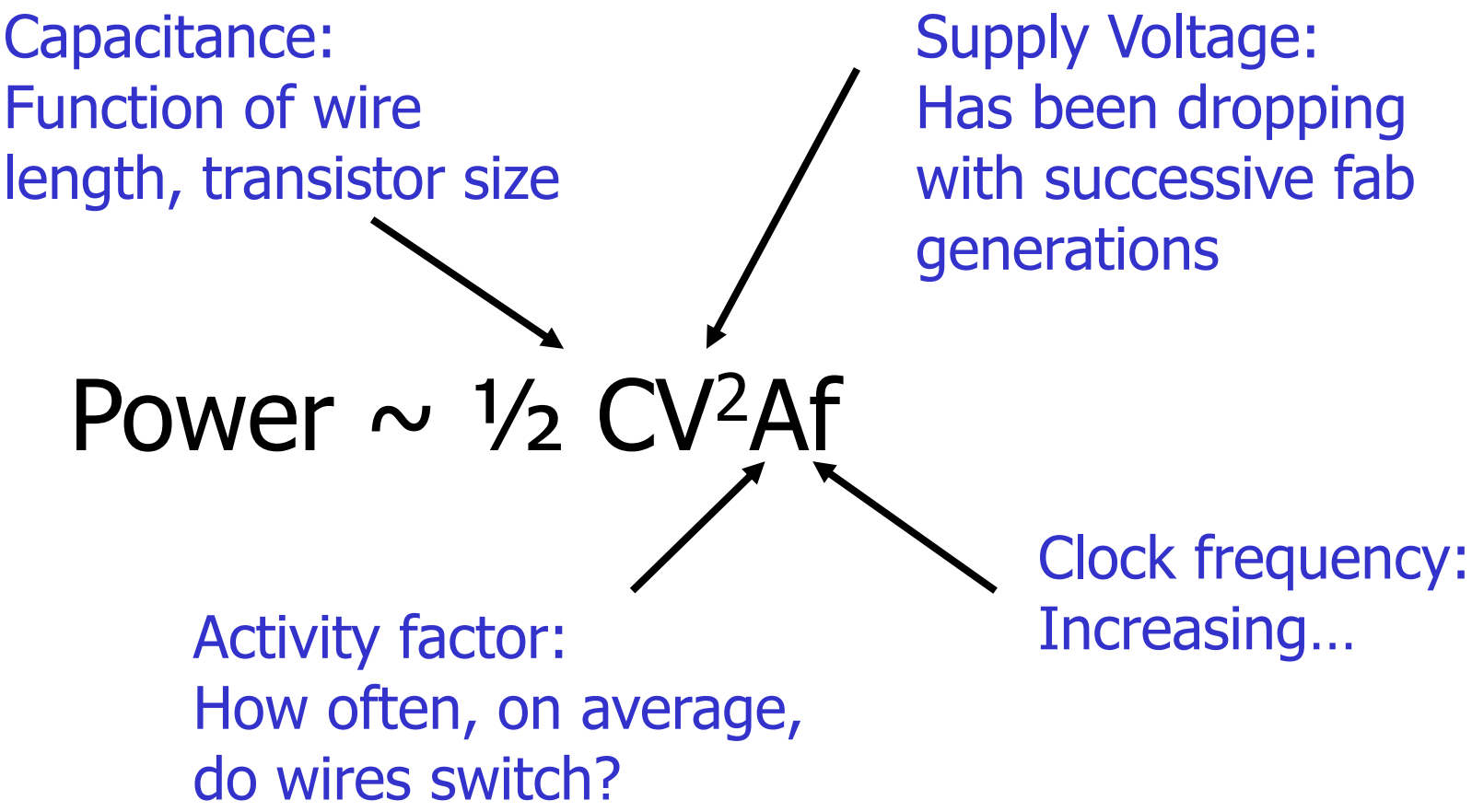





- **Data dependent – a function of switching activity**

# Capacitive Power dissipation





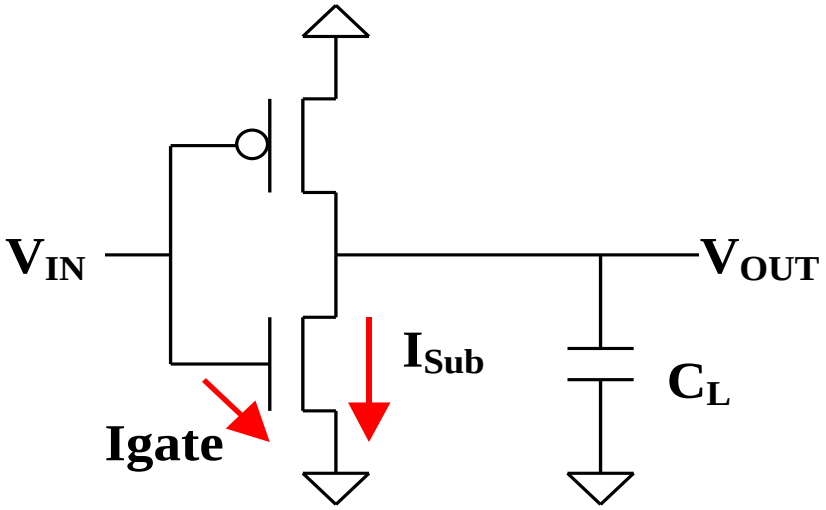
# Lowering Dynamic Power



- Reducing Vdd has a quadratic effect
  - Has a negative (~linear) effect on performance however
- Lowering $C_L$
  - May improve performance as well
  - Keep transistors small (keeps intrinsic capacitance (gate and diffusion) small)
- Reduce switching activity
  - A function of signal transition stats and clock rate
  - Clock Gating idle units
  - Impacted by logic and architecture decisions

# Static Power: Leakage Currents






$$I_{DSub} = k \cdot e^{\frac{-q \cdot V_T}{a \cdot k_a \cdot T}}$$

- Subthreshold currents grow exponentially with increases in temperature, decreases in threshold voltage
  - But threshold voltage scaling is key to circuit performance!
- Gate leakage primarily dependent on gate oxide thickness, biases
- Both type of leakage heavily dependent on stacking and input pattern

# Lowering Static Power



- **Design-time Decisions**
  - **Use fewer, smaller transistors -- stack when possible to minimize contacts with Vdd/Gnd**
  - **Multithreshold process technology (multiple oxides too!)**
    - **Use "high-Vt" slow transistors whenever possible**
- **Dynamic Techniques**
  - **Reverse-Body Bias (dynamically adjust threshold)**
    - **Low-leakage sleep mode (maintain state), e.g. XScale**
  - **Vdd-gating (Cut voltage/gnd connection to circuits)**
    - **Zero-leakage sleep mode**
    - **Lose state, overheads to enable/disable**

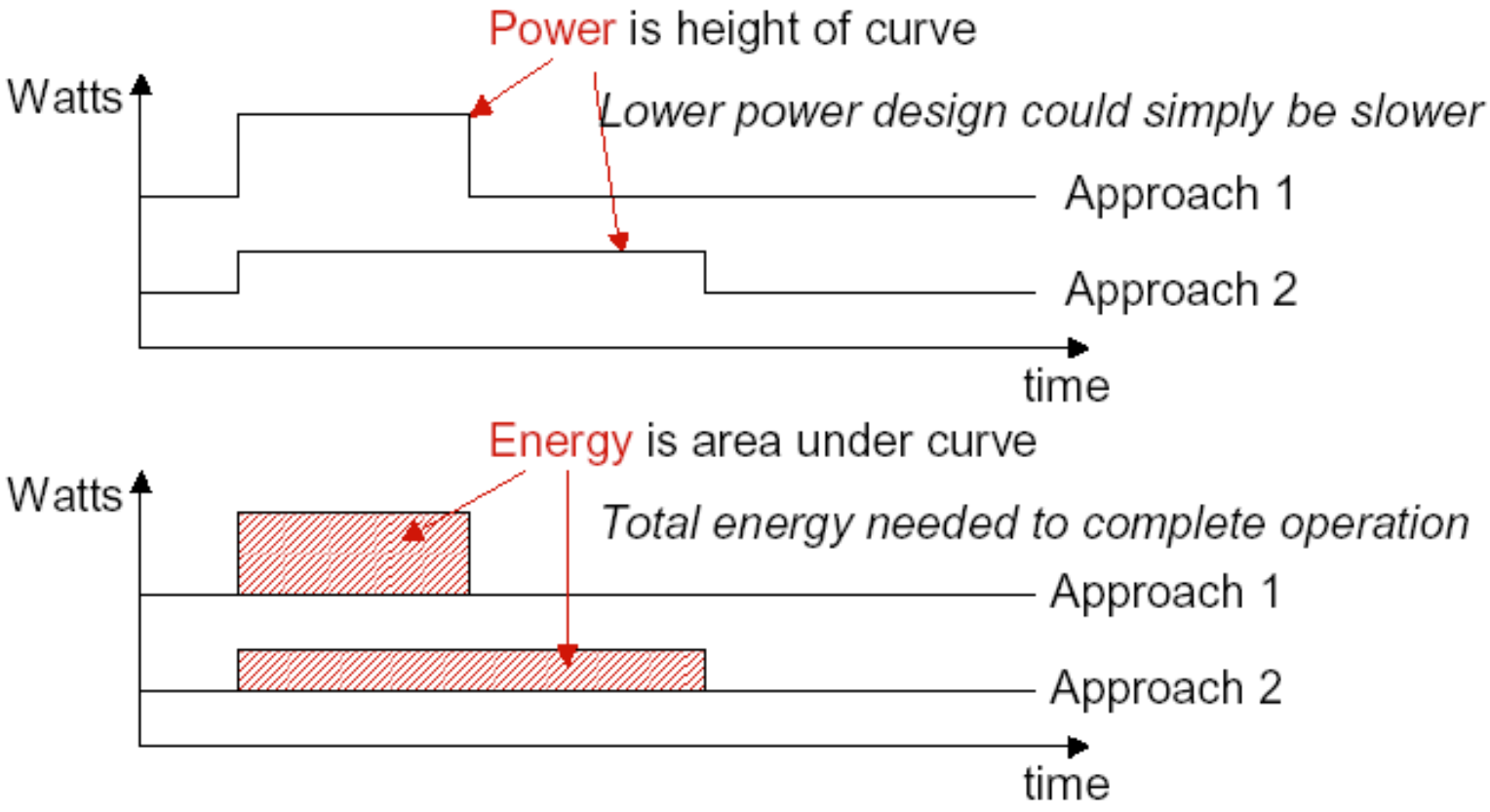
# Power vs. Energy



- **Power consumption in Watts**
  - **Determines battery life in hours**
  - **Sets packaging limits**
- **Energy efficiency in joules**
  - **Rate at which energy is consumed over time**
  - **Energy = power * delay (joules = watts * seconds)**
  - **Lower energy number means less power to perform a computation at same frequency**

# Power vs. Energy





# Power vs. Energy



- **Power-delay Product (PDP) = $P_{avg}$ * t**
  - **PDP is the average energy consumed per switching event**
- **Energy-delay Product (EDP) = PDP * t**
  - **Takes into account that one can trade increased delay for lower energy/operation**
- **Energy-delay$^2$ Product (EDDP) = EDP * t**
  - **Why do we need so many formulas?!!?**
  - **We want a voltage-invariant efficiency metric! Why?**
  - **Power ~ ½ $CV^2Af$, Performance ~ f (and V)**

# E vs. EDP vs. $ED^2P$



- Power ~ $CV^2f$ ~ $V^3$ (fixed microarch/design)
- Performance ~ f ~ V (fixed microarch/design)
- (For the nominal voltage range, f varies linearly with V)

- Comparing processors that can only use freq/voltage scaling as the primary method of power control:
  - $(perf)^3$ / power, or $MIPS^3$ / W is a fair metric to compare energy efficiencies.
  - This is an $ED^2$ P metric. We could also use: $(CPI)^3$ * W for a given application

# E vs. EDP vs. $ED^2P$



- **Currently have a processor design:**
  - **80W, 1 BIPS, 1.5V, 1GHz**
  - **Want to reduce power, willing to lose some performance**
  - **Cache Optimization:**
    - **IPC decreases by 10%, reduces power by 20% =>**
      **Final Processor: 900 MIPS, 64W**
    - **Relative E = MIPS/W (higher is better) = 14/12.5 = 1.125x**
  - **Energy is better, but is this a "better" processor?**

# Not necessarily



- 80W, 1 BIPS, 1.5V, 1GHz
  - Cache Optimization:
    - IPC decreases by 10%, reduces power by 20% => Final Processor: 900 MIPS, 64W
    - Relative E = MIPS/W (higher is better) = 14/12.5 = 1.125x
    - Relative EDP = $MIPS^2/W$ = 1.01x
    - Relative $ED^2P$ = $MIPS^3/W$ = .911x
- What if we just adjust frequency/voltage on processor?
  - How to reduce power by 20%?
  - $P = CV^2F = CV^3$ => Drop voltage by 7% (and also Freq) => .93*.93*.93 = .8x
  - So for equal power (64W)
    - Cache Optimization = 900MIPS
    - Simple Voltage/Frequency Scaling = 930MIPS