EECS 470 Quiz, Fall 2009. Closed book/closed notes!

Name: _____ Uname: _____
You have 20 minutes for this quiz. The quiz is closed notes/closed book. If you should finish early, you are welcome to turn in your quiz and step out of the room until the lecture starts. **There are 2 pages to this quiz and it is graded out of 30 points.**

I have neither given nor received aid on this quiz, nor observed anyone else doing so.

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1) Short answer
   a) Consider the following access pattern***: A, B, C, D, E, A***. Assume that A, B, C, D and E are memory addresses each of which are in a different block of memory. Further, assume A, B, C, D and E are generated in a uniformly random way and that a "true" LRU replacement algorithm is used. What is the probability that the second instance of "A" will be a hit if:

      i) Cache is an 8-line direct-mapped cache? **[4]**

      ii) Cache is a 4-line fully associative cache? **[4]**

2) Say you are working on a processor which is being targeted for portable application. The only thing the processor does is run a program once every 1000 seconds that consists of executing 10^{11} instructions with a near-100% cache hit rate. When the processor is idle (not running the program) it uses 10mW of power. When it is active, it uses 4W of power. The processor can execute the program at a rate of 10^9 instructions per second (so it takes 100 seconds to run the program).
   a) What is the *average* power consumption of this processor running as described above? **[3]**

   b) Your boss has asked you to estimate what the average power consumption would be if you used voltage scaling to drop the voltage to 80% of what it currently is. *Clearly* show your work. **[5]**

3) Consider a case of having 3 processors using a snoopy MESI protocol where the memories can snarf data. All three have a 2 line direct-mapped cache with each line consisting of 16 bytes. The caches begin with all lines marked as invalid. Fill in the following tables indicating
   - If the processor gets a hit or a miss in its cache
   - If a HIT or HITM (or nothing) occurs on the bus during snoop.
   - What bus transaction(s) (if any) the processor performs (BRL, BWL, BRIL, BIL)
   - For misses only, indicate if the miss is compulsory, capacity, conflict, or coherence. A coherence miss is one where there would have been a hit, had some other processor not caused an invalidation of that line.

   In the event more than one bus transaction occurs due to a given memory read/write indicate the response for each bus transaction. Finally, indicate the state of the processor after all of these memory operations have completed. The operations occur in the order shown. **[14 points, -0.5 per wrong or blank, minimum of 0]**

Processor	**Address**	**Read/Write**	**Bus transaction(s)**	**Hit/Miss**	**HIT/ HITM**	**"4C" miss type (if any)**
1	0x200	Read				
1	0x210	Write				
1	0x110	Read				
1	0x210	Read				
1	0x200	Write				
2	0x210	Read				
2	0x200	Write				
1	0x200	Read				

Final state:

	Proc 1	
	Address	**State**
Set 0		
Set 1		

	Proc 2	
	Address	**State**
Set 0		
Set 1		