Name: _____ Uname: _____

You have 25 minutes for this quiz. The quiz is closed notes/closed book. If you should finish early, you are welcome to turn in your quiz and step out of the room until the lecture starts. **There are 2 pages to this quiz.**

I have neither given nor received aid on this quiz, nor observed anyone else doing so.

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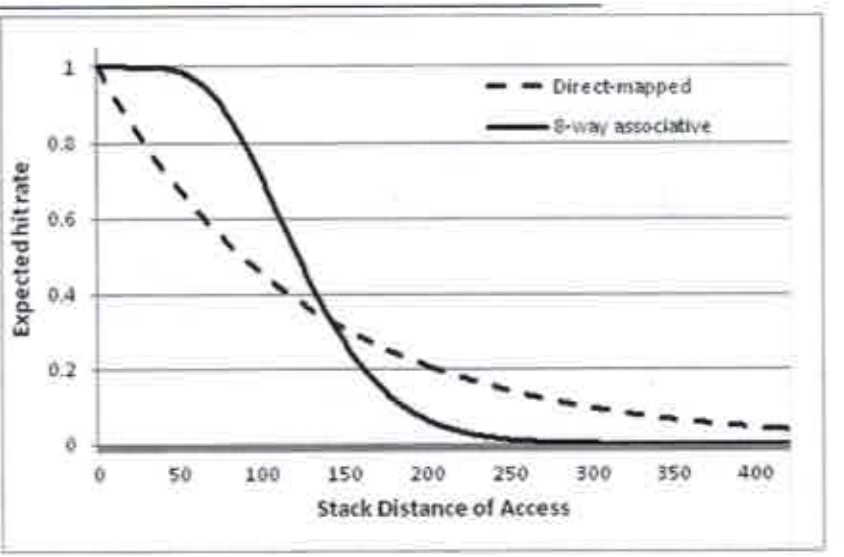
1. In the graph to the right, we see the expected hit rate of a memory access with a given stack distance for two caches with the same number of lines (128) but different degrees of associativity. Both lines have the same area under the curve (again, 128). Using this graph, ***briefly*** explain why more associative caches tend to get higher hit rates than less associative caches. **[8 points]**



2. Consider the following access pattern: A, B, C, A. Assume that A, B, and C are memory addresses each of which are in a different block of memory. Further, assume A, B and C are generated in a uniformly random way and that a "true" LRU replacement algorithm is used. Further, assume that any given block has an equal chance of being placed in either "way" if both blocks are invalid. To receive credit you must show your work. **[7 points]**

   What is the probability he the second instance of "A" will be a hit if:

   a. The cache has 8 lines (total) and is a two-way associative cache **[2]**

   b. The cache has 8 lines (total) and is a two-way associative skew cache **[5]**

3. Consider a case of having 3 processors using a snoopy MESI protocol where the memories can snarf data. All three have a 2 line direct-mapped cache with each line consisting of 16 bytes. The caches begin with all lines marked as invalid. Fill in the following tables indicating
   - If the processor gets a hit or a miss in its cache
   - If a HIT or HITM (or nothing) occurs on the bus during snoop.
   - What bus transaction(s) (if any) the processor performs (BRL, BWL, BRIL, BIL)
   - For misses only, indicate if the miss is *compulsory, capacity, conflict, or coherence.* A coherence miss is one where there would not have had to create a bus transaction had some other processor not caused an invalidation of that line.

In the event more than one bus transaction occurs due to a given memory read/write indicate the response for each bus transaction. Finally, indicate the state of the processor after all of these memory operations have completed. The operations occur in the order shown. **[15 points, -0.5 per wrong or blank, minimum of 0]**

Processor	Address	Read/ Write	Cache Hit/Miss	Bus transaction(s)	HIT/ HITM	"4C" miss type (if any)
1	0x100	Read				
1	0x210	Write				
1	0x200	Read				
1	0x100	Read				
1	0x140	Write				
2	0x200	Read				
1	0x100	Write				
1	0x210	Write				
3	0x120	Write				
1	0x310	Read				

Final state:

	Proc 1	
	Address	State
Set 0		
Set 1		

	Proc 2	
	Address	State
Set 0		
Set 1		

	Proc 3	
	Address	State
Set 0		
Set 1		

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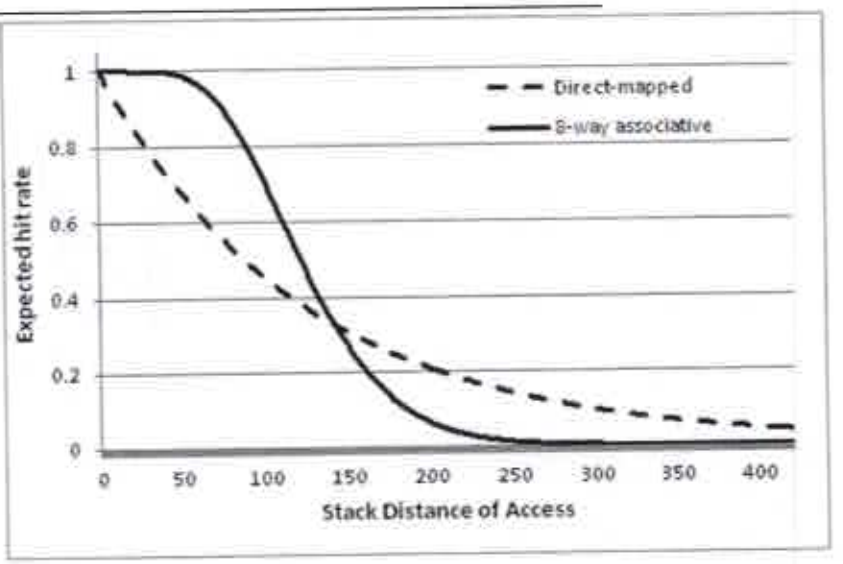

As can be seen, associative caches get a higher hit rate on low stack distances. Because most programs have significant temporal locality, we expect most programs to have a high percentage of fairly low stack distance accesses. Thus the associative cache will get a better hit rate.

2. Consider the following access pattern: A, B, C, A. Assume that A, B, and C are memory addresses each of which are in a different block of memory. Further, assume A, B and C are generated in a uniformly random way and that a "true" LRU replacement algorithm is used. Further, assume that any given block has an equal chance of being placed in either "way" if both blocks are invalid. To receive credit you must show your work. **[7 points]**

What is the probability he the second instance of "A" will be a hit if:

a. The cache has 8 lines (total) and is a two-way associative cache **[2]**

$1 - (1/4)\cdot(1/4) = 15/16$

B+C go to same set as A.

b. The cache has 8 lines (total) and is a two-way associative skew cache **[5]**

A: Put B goes to different way $= \left(\frac{1}{4}\right)\cdot 1 + \frac{3}{4}\cdot 1/2 = 1/4 + 3/8 = 5/8$

B: C conflicts with A+B $= 1/16$

$1 - \left(\frac{5}{8}\cdot\frac{1}{16}\right) = 123/128$

3. Consider a case of having 3 processors using a snoopy MESI protocol where the memories can snarf data. All three have a 2 line direct-mapped cache with each line consisting of 16 bytes. The caches begin with all lines marked as invalid. Fill in the following tables indicating
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Processor	Address	Read/ Write	Cache Hit/Miss	Bus transaction(s)	HIT/ HITM	"4C" miss type (if any)
1	0x100	Read	MISS	BRL	–	CUMP
1	0x210	Write	MISS	BRIL	–	CUMP
1	0x200	Read	MISS	BRL	–	CUMP
1	0x100	Read	MISS	BRL	–	CAP
1	0x140	Write	MISS	BRIL	–	CUMP
2	0x200	Read	MISS	BRL	–	CUMP
1	0x100	Write	MISS	BRIL/BWL	–	conflict
1	0x210	Write	Hit	–	–	/
3	0x120	Write	MISS	BRIL	–	CUMP
1	0x310	Read	MISS	BRL/BWL	–	CUMP

Final state:

	Proc 1	
	Address	State
Set 0	0x100	M
Set 1	0x310	E

	Proc 2	
	Address	State
Set 0	0x200	E
Set 1		

	Proc 3	
	Address	State
Set 0	0x120	M
Set 1		