Name: _____ Uname: _____

You have 20 minutes for this quiz. The quiz is closed notes/closed book. If you should finish early, you are welcome to turn in your quiz and step out of the room until the lecture starts. **There are 2 pages to this quiz.**

I have neither given nor received aid on this quiz, nor observed anyone else doing so.

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1. Consider the following access pattern: A, B, C, B, A. Assume that A, B, and C are memory addresses each of which are in a different block of memory. Further, assume A, B and C are generated in a uniformly random way.
    a. What is the probability that the second instance of "B" will be a hit on a 4-line direct-mapped cache? Briefly show your work. **[10]**

    b. What is the probability that the second instance of "A" will be a hit on a 4-line 2-way associative cache? Again, briefly show your work. **[15]**

2. A coworker has been testing a new low-power computing platform to replace your company's current platform. She claims that "This thing is junk. It is low power, but it's higher energy to run each job!"
    a. _Briefly_ explain how it is possible that it could be lower power and yet higher energy. **[10]**

    b. Given what you know of the relationship between power and performance, is she right to call it "junk"? Explain your answer in 30 words or less. **[15]**

3. Consider a case of having 3 processors using a snoopy MESI protocol where the memories can snarf data. All three have a 2-line direct-mapped cache with ***each line consisting of 8 bytes***. The caches begin with all lines marked as invalid. Fill in the following tables indicating
   - If the processor gets a hit or a miss in its cache
   - If a HIT or HITM (or nothing) occurs on the bus during snoop.
   - What bus transaction(s) (if any) the processor performs (BRL, BWL, BRIL, BIL)
   - For misses only, indicate if the miss is compulsory, capacity, conflict, or coherence. A coherence miss is one where there would have been a hit, had some other processor not interfered.

Finally, indicate the state of the processor after all of these memory operations have completed. The operations occur in the order shown. **[50 points, -2 per wrong or blank, minimum of 0]**

Processor	Address	Read/Write	Cache Hit/Miss	Bus transaction(s)	HIT/ HITM	"4C" miss type (if any)
1	0x100	Read	Miss	BRL	—	compulsory
1	0x008	Write	Miss	BRIL	—	compulsory
1	0x018	Read	Miss	BWL, BRL	—	conflict
1	0x107	Write	Hit	—	—	—
2	0x100	Read	Miss	BRL	HITM	compulsory
2	0x100	Write	Hit	BIL	HIT	—
2	0x01F	Write	Miss	BRIL	HIT	compulsory
1	0x018	Read	Miss	BRL	HITM	coherence
3	0x100	Read	Miss	BRL	HITM	compulsory
1	0x100	Read	Miss	BRL	HIT	coherence

Final state:

Proc 1

	Tag .	State
Set 0	0x10	S
Set 1	0x01	S

Proc 2

	Tag .	State
Set 0	0x10	S
Set 1	0x01	S

Proc 3

	Tag .	State
Set 0	0x10	S
Set 1		I