A 5.2GHz RF Front-End

Neel Natekar, Vasudha Vasudevan, and Anupam Viswanath, *University of Michigan, Ann Arbor.*

***Abstract*—A 5.2 GHz radio frequency receiver front-end employing a dual down-conversion heterodyne architecture suitable for use with the IEEE802.11a standard is proposed in IBM 0.13 um CMOS technology. The design achieves high image rejection and uses noise and gain optimization techniques in mixer design. An overall voltage conversion gain of 35.3 dB, a noise figure of 9.8 dB and image rejection of 57.1 dB are achieved with a power consumption of 20.6 mW from a 1.2 V supply. Circuit simulation was performed and the circuit was laid out using Cadence® Virtuoso® tools.**

***Index Terms*—dual down-conversion heterodyne, IEEE 802.11a, in-built image rejection, optimized mixer design, receiver front end**

I. Introduction

The demands of the growing wireless communication industry have triggered an intensive effort to design transceivers with low power consumption, low cost and small form factor.[1] CMOS technology scaling allows for the design of highly integrated systems with low cost including for 5 GHz radio frequency (RF) applications.[2]

The 5 GHz RF band is attractive for wireless communication applications because it has hundreds of megahertz of unlicensed spectrum and is unaffected by interference from microwave oven radiations, unlike the 2.4-GHz band. The IEEE802.11a and the HIPERLAN standards have both been designated for operation in this band. These standards support data rates of upto 54 Mb/s making them attractive for data-intensive applications.

A 5.2 GHz CMOS receiver suitable for use with the IEEE802.11a standard is described in this paper. The receiver employs a double down-conversion heterodyne architecture and achieves high image rejection without the need for external components. A low-noise amplifier, two down-converting mixers and a baseband amplifier have been designed. Each block has been individually designed to meet the overall system requirements of high conversion gain, low noise figure, high image rejection, linearity and low power consumption.

II. Receiver Architecture

The receiver architecture and frequency planning have been designed as recommended for use with the IEEE802.11a. This standard requires a receiver with a noise figure of <10dB and a high image rejection.

The receiver architecture is shown in Figure 1. The circuit consists of a low noise amplifier (LNA) and performs two down-conversions both using a local oscillator frequency of 2.6 GHz. The input RF signal is thus frequency translated from 5.2 GHz to 2.6 GHz and finally to zero. This baseband signal is then filtered and amplified.

The architecture uses coupling capacitors between the LNA and the mixers to eliminate flicker noise and to decouple the dc levels at the output and input of the blocks, allowing us to maximize the operation of each block.

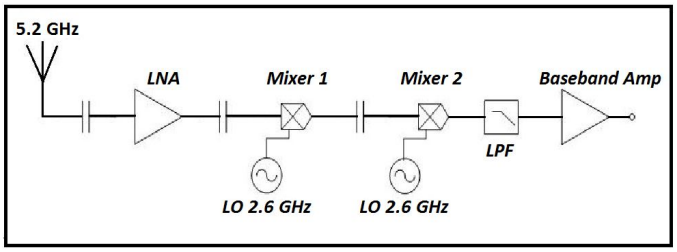

Figure 1. Receiver Architecture

In this frequency plan, the frequency synthesizers or oscillators operate at half the input frequency. This imposes less stringent requirements on the oscillators and more accurate quadrature phases may be obtained. Further, the image band is now centered at zero frequency and as a result, is greatly attenuated by the antenna and the LNA, eliminating the need for explicit image rejection filters.[3] This also makes the receiver more amenable to system integration.[1]

This receiver architecture however must deal with three issues. The flicker noise in the LNA and the input transistors of the first RF mixer are up-converted to the first IF leading to possible signal corruption. Also, any LO-IF feed-through from the RF mixer lies at the first IF, desensitizing the second IF mixer. Thirdly, since there is no channel-selection filter between the two mixers, the second mixer should have a high linearity. These issues are taken into consideration in designing the building blocks of the receiver.

III. Design, Analysis and Simulation of the Building Blocks

A. LNA

The first stage of the front-end, the LNA significantly affects the overall front-end performance and has to satisfy stringent requirements with respect to noise figure, power matching and gain. To operate within the limited frequency spectrum standardized for IEEE 802.11a WLAN applications, the LNA should have a narrow band centered around 5.2 Ghz with a pass-band not greater than 40 MHz. Also, the LNA should be designed to burn as little power as possible. In order to achieve all the above mentioned requirements, an

inductively degenerated cascoded common-source amplifier topology was chosen as shown in Figure 2.

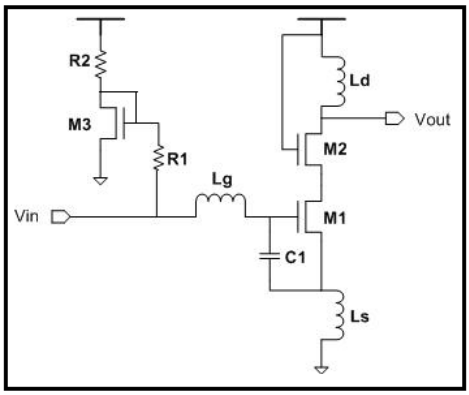

Figure 2. LNA Schematic

This is a widely used topology in narrow band designs[4]. In this topology the input network of the amplifying device is embedded in a reactive network so that the overall input reactance is resonated at a particular bandwidth. Various techniques exist which enable this narrow-band LNA to act as multiband concurrent LNAs[5]. In this way a wide band input match is achieved and at the same time a good noise performance is attained. It has been shown in literature that for MOS devices, noise match is very close to power match [4].

The design methodology used to calculate the optimum bias current and input transistor M1 parameters is as follows. Plots of g_{m_den},g_{do_den},$\alpha = g_m/g_{do}$, C_{gs_den} and $\omega_t = g_m/C_{gs}$ versus I_{den} where used, to choose a value of I_{den} that would provide sufficient trans-conductance while maintaining low power consumption. A plot of Noise Factor (NF) against Q_{in} was then used to calculate C_{gs}, g_m and I_{ds} through the transistor. The various equations used in this analysis were:

$$F = 1 + \left[\frac{\omega_0}{\omega_t}\right]\frac{\gamma}{\alpha 2Q}\{1 - 2.|c|.\chi_d + (4Q^2 + 1)\chi_d^2\} \quad \text{.... (1)}$$

Where $\alpha = g_m/g_{do}$, $\chi_d = \alpha\sqrt{\delta/5\gamma}$ and c is the gate noise correlation coefficient assumed to be - j0.55.

$$\text{Also } Q_{in} = \frac{1}{2\omega_0 C_{gs} R_s} \quad \text{.... (2)}$$

The cascode configuration used improves the input-output reverse isolation and the frequency response of the amplifier. To Bias M1, a current mirror topology was used comprising of $M3_3$, $R1_1$ and $R2_3$.

The source degeneration inductor, Ls is used to tune the amplifier input resistance to that of the source (Rs). An Inductor (Lg) is also placed in series with the gate providing an additional degree of freedom to set the resonating frequency, ω_o. Since inductors occupy significant amounts of area in any RF circuit layout, to minimize their sizes a third degree of freedom was added in the form of C1, a capacitor across the gate of $M1_1$. The Inductive load Ld was tuned to resonate at the required operational frequency of 5.2 Ghz.

The equations for power matching and for calculating Lg using the center resonant frequency are respectively,

$$R_s = \frac{g_m L_s}{C_{gs} + C_1} \quad \text{.... (3)}$$

$$\omega_o^2 = \frac{1}{(L_g + L_s)(C_{gs} + C_1)} \quad \text{.... (4)}$$

Tradeoffs involved in this design were primarily between gain, noise figure and linearity. NF decreases with increase in current I_{ds}. However this can be done only to an extent so as to preserve input matching of the LNA. Also $P1_{db}$ varies inversely as a function of I_{ds} and hence the Gain- Linearity tradeoff. In this LNA design, the requirement for high gain superseded that of high linearity , but a sufficient amount of linearity is still required.

The simulated performance parameters of the LNA are as tabulated in Table 1.

Table 1. LNA Performance

Noise Figure	1.58 dB
Gain and P1db	29.82 dB Gain at -31 db P1dB
Gain and P1db	17.30 dB Gain at -8 db P1dB
Power	7.61 mW

B. RF-Mixer

The down conversion mixer is one of the most important building blocks for RF transceivers in wireless communications, their performance often constraining the performance of the RF front ends.

The RF mixer downconverts the RF signal (5.2 Ghz) amplified by the LNA to the desired intermediate frequency (IF) of 2.6 Ghz. A double balanced gilbert cell topology was chosen because it has very low LO-IF feed-through and performs cancellation of even harmonics. The RF Mixer schematic is shown in Figure 3.

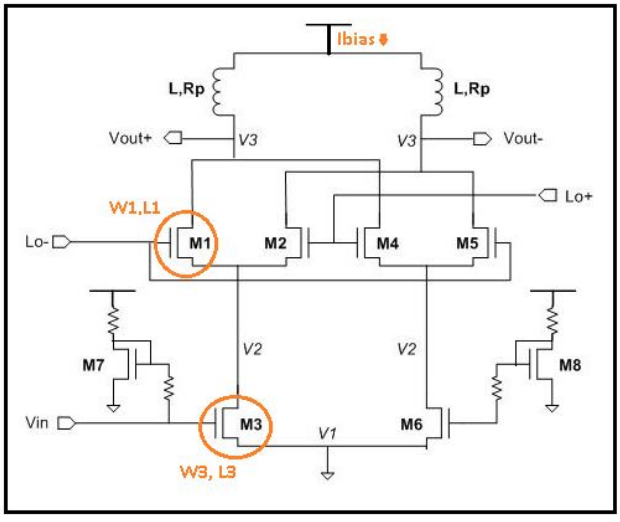

Figure 3. RF Mixer Schematic

In this schematic the output from the LNA is AC coupled to the RF input transistors M3, M6. These transistors are biased using a current mirror topology comprising of transistors M7, M8. The switching transistors M1,2,4,5 act as current steering switches. It can be seen that the drain-source voltages of all FETs are determined by node voltages V_1, V_2 and V_3. Thus, for a given supply voltage, bias current the transistor operating regions can be set by adjusting bias levels of the input or local oscillator (LO), load and aspect ratios of M1-M6.

To select appropriate values for the aspect ratios of M1-M6 to ensure optimum noise performance and conversion gain, a preliminary analysis was performed using MATLAB. The equations for Noise Figure (NF) and conversion gain (CG) as a function of mixer parameters have been shown to be[6]:

$$NF_{(SSB)} = 10.LOG\left[\frac{\alpha}{c^2} + \frac{2(\gamma_3 + rg_3.g_{m3})\alpha.g_{m3} + \gamma_1\overline{G} + (4r_{g1})\overline{G^2} + \left(\frac{1}{R_L}\right)}{R_S.c^2(g_{m3})^2}\right] \quad \text{.... (5)}$$

$$CG = A_{VRF} \times A_{switch} = -\frac{2}{\pi} g_{m3}.(r_{ds1} // R_L) \quad \text{.... (6)}$$

where G=2. g_{m1}. g_{m2}/(g_{m1}+ g_{m2}).

It can be seen that NF and CG are functions of the trans-conductance of transistors M1 and M3 which are in turn functions of the transistor aspect ratios. Simulations were run in MATLAB and the plots obtained for NF, CG vs (W_3 and W_1) are shown in Figures 4 and 5 respectively.

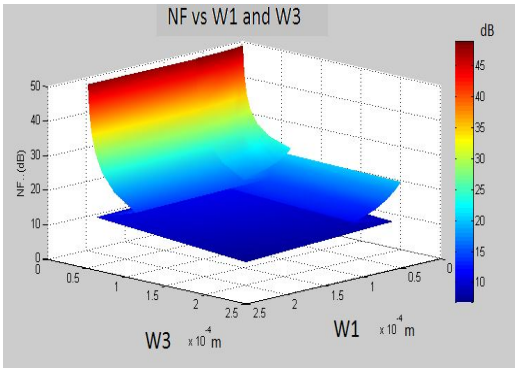

Figure 4. Plot of Noise Figure vs. (W1,W3)

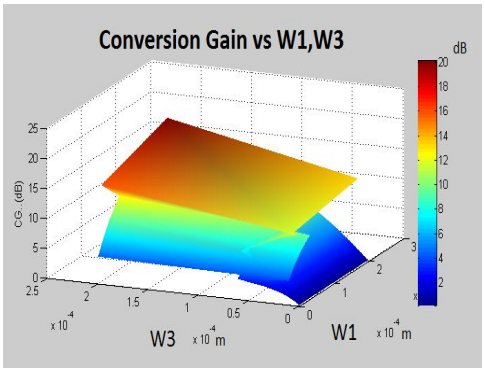

Figure 5. Plot of Conversion Gain vs. (W1,W3)

As seen in the plot the NF reduces for increase in W_1 and W_3 as expected, but this reduction is significantly more for the increase in W_3 than W_1. Using plots from Figures 4-5, optimum parameters for RF and switching transistors as well as optimum biasing points were chosen to ensure good noise figure and conversion gain turnout.

The variation of conversion gain, LO –IF feed-through, etc versus the LO power was studied and a LO power of 8dBm was chosen. In choosing this value primarily three design criteria were considered. The LO power was chosen to not be so large as to increase LO-RF feed-through, increase LO-IF feed-through thus desensitizing the second mixer and make the LO design complex.

Figure 3 shows the use of inductors as load in place of resistors which is possible because of the high IF frequency (2.6 GHz) which reduces the thermal noise in circuit. Also since there is negligible DC drop across inductors the available headroom across LO and RF transistor increases. However this choice comes at the cost of additional area.

The load inductor value is chosen so that inductor provides a high parallel resistance Rp around 5.2 GHz, maximizing the voltage gain. The load inductance also affects the LO-IF feed-through and thus is chosen appropriately keeping in mind the inherent tradeoff between gain and feed-through.

One of the challenges in this receiver architecture is the upconversion of Flicker Noise of the LNA and the input stage of the first mixer to the first IF (2.6 GHz). In order to minimize this problem coupling capacitors were used between LNA and the RF mixer and the transistors were upsized so as to reduce the flicker noise corner frequency. An alternate topology has been suggested for the reduction of this flicker noise [3] and is shown in Figure 6.

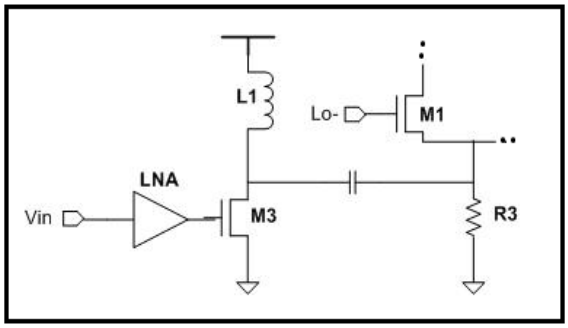

Figure 6. Portion of RF Mixer Schematic showing alternate topology

In this scheme the RF input transistor is removed from the stack and then capacitively coupled to the stack, which minimizes the amount of flicker noise being upconverted. The reduction in flicker noise with this alternate topology is shown in Figure 7.

This scheme however also has some disadvantages. First, the two additional inductors increase the circuit area significantly. Second, power dissipation increases since current drawn from supply increases. Thirdly, this also requires a DC level compatibility between the output of the LNA and the input to the mixer. Also, as can be seen from

figure the introduction of additional resistors increases thermal noise.

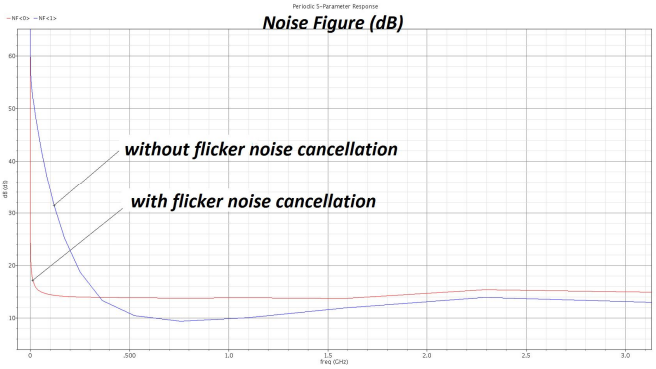

Figure 7. Noise Figure variation with alternate topology

Thus, the RF mixer was designed and its simulated performance metrics are listed in Table 2.

Table 2. RF Mixer Performance

Gain	9.5 dB
Noise Figure	17 dB
IIP3	-10 dBm
P1 dB	-19 dBm
Power	7.4 mW

C. IF Mixer

The second downconversion mixer, i.e. the IF mixer is similar in structure to the first mixer. It down converts the input signal at 2.6 GHz to zero frequency. It is also designed using a double balanced gilbert cell topology and designed keeping in mind the optimization scheme as obtained from the analysis of Figures 4-5.

The input transistors of the fully differential mixer are of the grounded source type and it uses a resistive load at the top of stack. The schematic of the IF mixer designed is shown in Figure 8.

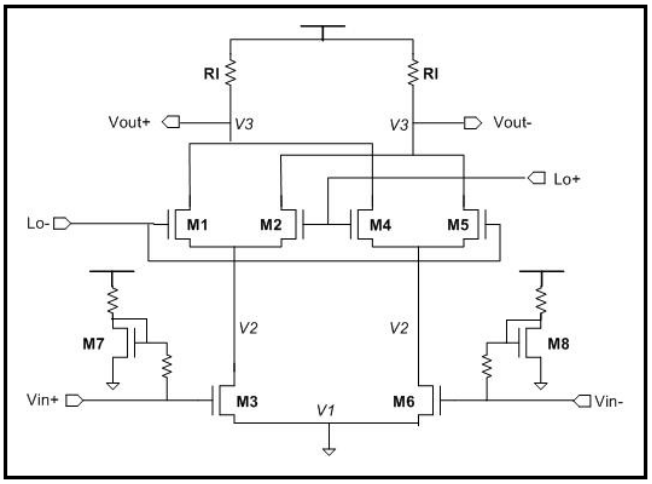

Figure 8. IF Mixer Schematic

The major design criteria for the IF mixer is high linearity which trades off directly with noise figure and conversion gain. Linearity is especially important because there is no channel filtering at the high frequency of 2.6 GHz between the two mixers.

The mixer optimized to produce reasonable gain, low NF and high linearity, while consuming low power has performance parameters as shown in Table 3, wherein its performance is compared very favorably to other published work in recent years.

Table 3. IF-Mixer Performance and Benchmarking

Parameter	[7]	[8]	[9]	Our Work
Technology (μm)	0.18	0.5	0.25	0.13
Supply Voltage (V)	1.5	2.5	1.8	1.2
Conversion Gain (dB)	3.3	3.35	-2.688	6
P1 (dBm)	-8.98	-8.2	5.075	-2.9
IIP3 (dBm)	5.46	2.17	12.81	5.57
Noise Figure (dB)	14.87	9.04	13.67	13.2
Power (mW)	5.6	10	13.3	5.04

D. Baseband Amplifier

Once the signal is downconverted to the baseband it must be filtered, amplified and digitized, but these steps maybe performed in any order[1]. In this receiver front-end design, a baseband amplifier for use as the first stage of baseband processing is designed and it is thus required to have a high linearity. A fully differential NMOS amplifier is designed and the schematic is shown in Figure 9. The amplifier performance metrics are shown in Table 4.

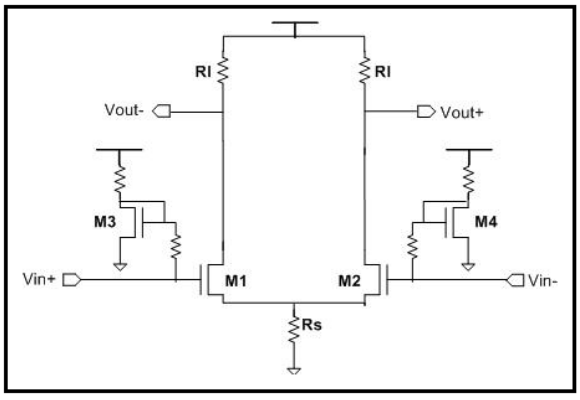

Figure 9. Baseband Amplifier Schematic

Table 4. Baseband amplifier Performance

Gain	3.2 dB
Noise Figure	9.2 dB
P1 dB	7.5 dBm
Power	0.57 mW

As shown here, it achieves a high 1-dB compression point value of 7.5 dBm which limits its voltage gain to 3.2 dB. These values are appropriate because as previously explained, high linearity is a more stringent requirement at this stage and additional gain can be obtained during further baseband processing.

IV. Simulation Results

The overall receiver system consisting of the LNA, mixers and the baseband amplifier blocks designed as discussed above, is put together as depicted in Figure 1 and simulated. The simulation results are summarized and benchmarked in Table 5.

Table 5. Overall Performance

Parameter	Razavi[3]	Our work
Technology (μm)	0.25	0.13
Supply Voltage (V)	2.5	1.2
Center frequency (Ghz)	5.2	5.2
Noise figure (dB)	6.4	9.83
1 dB Compression (dBm)	-26.5	-36.5
Image rejection (dB)	62	57.1
Voltage Gain (dB)	43	35.28
Power dissipation (mW)		
LNA	8.75	7.61
RF Mixer	5	7.4
IF Mixer	5	5.04
Baseband section	5.25	0.57
Total	29	20.62

As shown here our work achieves comparable voltage gain and image rejection with previously reported work. Image rejection achieved using conventional Hartley or Weaver architectures are 30-40 dB and our work achieves a much greater 57.1dB rejection. Also, even though our noise figure is higher than previous work, this value can still be tolerated by our target application. We however achieve much lower power dissipation than previous work.

V. Layout

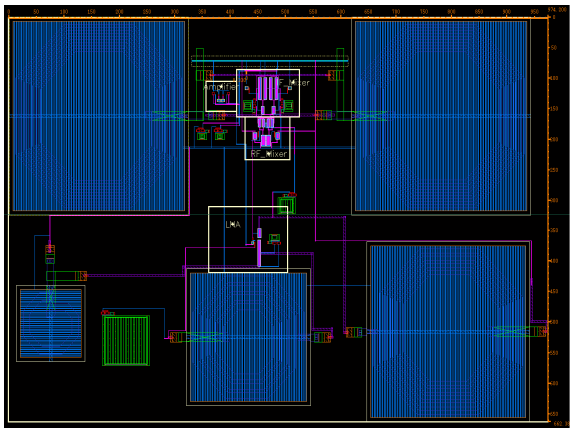

Figure 10. Layout

The complete circuit is laid out using the Cadence Virtuoso layout editor. Care was taken to minimize coupling between the inductors, to maintain symmetry in the layout and minimize the area. Area of layout is 0.974 μm x 0.662 μm.

VI. Conclusion

A 5.2 GHz RF receiver front-end suitable for use with the IEEE802.11a standard has been designed using IBM 0.13 um CMOS technology. The receiver employs a dual conversion heterodyne architecture and uses noise and gain optimization techniques in mixer design. An overall voltage conversion gain of 35.3 dB, a noise figure of 9.8 dB and a high image rejection of 57.1 dB have been achieved while maintaining a low power consumption of 20.6 mW from a 1.2 V supply.

Further work in this project may include the design of the frequency synthesizers to generate 2.6 GHz LO frequencies and the design of robust dc offset cancellation techniques for the baseband amplifier.

References

[1] Razavi, B.; , "Design considerations for direct-conversion receivers," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on , vol.44, no.6, pp.428-435, Jun 1997

[2] Ong, H.K.F.; Yeung Bun Choi; Wooi Gan Yeoh; , "A Variable Gain CMOS RF front-end for 5 GHz Applications," Radio-Frequency Integration Technology, 2007. RFIT 007. IEEE International Workshop on , vol., no., pp.314-317, 9-11 Dec. 2007

[3] Razavi, B.; , "A 5.2-GHz CMOS receiver with 62-dB image rejection," Solid-State Circuits, IEEE Journal of , vol.36, no.5, pp.810-815, May 2001

[4] T. H. Lee, The Design of CMOS Radio-Freqency Integrated Circuits, 1st ed. New York: Cambridge Univ. Press, 1998

[5] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers—Theory, design, and applications," IEEE Trans. Microwave Theory Tech., vol. 50, pp. 288–301, Jan. 2002.

[6] "Design Optimization Methodology of CMOS Active Mixers for Multi-Standard Receivers " S. Douss, F. Touati and M. Loulou,2007

[7] Hung-Che Wei, Ro-Min Weng, Chih-Lung Hsiao and Kun-Yi Lin, " A 1.5V,2.4Ghz CMOS Mixer With High Linearity", The 2004 IEEE Asia-Pacific Conference Circuit and Systems , Dec 6-9, 2004

[8] H.Kilicaslan, H.S Kim, and M.Ismail ,"A 1.9Ghz CMOS down-conversion mixer ",Proc. 40th Midwest Symp. Circuit System, vol2 pp.1172-1174, 1998

[9] Kumar Munusamy and Zubaida Yusoff ," A Highly Linear CMOS Down Conversion Double Balanced Mixer", ICSE2006 Proc. 2006, Kuala Lumpur, Malaysia