Shantanu Gupta

www.eecs.umich.edu/∼shangupt

2260 Hayward St. #4861, Ann Arbor, MI 48105, Ph: *734-276-3331* shangupt@umich.edu

RESEARCH INTERESTS

Architecture and Compiler level solutions for Fault Tolerance (transient and hard faults), Performance, Energy-efficiency, and Concurrency bugs.

EDUCATION

University of Michigan, Ann Arbor May 2007 - present
Ph.D. in Computer Science and Engineering (*Expected: April, 2011*)
Thesis Title: *Adaptive Architectures for Robust and Configurable Performance*
Advisor: Prof. Scott Mahlke

University of Michigan, Ann Arbor Sep 2005 - Apr 2007
M.S.E in Computer Science and Engineering
GPA: 8.0 / 9.0

Indian Institute of Technology, Guwahati May 2001 - May 2005
B. Tech in Computer Science and Engineering
GPA: 9.5 / 10.0 (*Institute Rank: 1*)

EXPERIENCE

University of Michigan, Ann Arbor May 2006 - Present
Graduate Student Research Assistant, Department of EECS
Design of adaptive multicore architectures for reliability, performance, and energy efficiency.

Reliability: My reliability research efforts have covered various aspects of soft and hard error tolerance including prevention, detection, repair and recovery. A fundamental contribution here was the design of a highly reconfigurable computing substrate, named StageNet, that can perform pipeline-stage level fault isolation in multicore chips. The original idea and its extensions appear in CASES'08, MICRO'08, and DSN'10.

Performance: A follow-up to the StageNet project, named CoreGenesis, builds upon the architectural flexibility to provide a unified performance-reliability solution. The objective here was to harness architectural flexibility (in StageNet-like architectures) for customizing processors to workloads. This customization can be for pipeline-width (narrow and wide issue processors), number and types of functional units, cache configuration, etc. An instance of the CoreGenesis vision appears in MICRO'10.

Energy-Efficiency: My current focus is to design energy-efficient compute engines for general purpose applications. The insight here is to cut down on the redundant instruction fetch, decode and register file access energy by optimizing the execution of recurring instruction sequences.

Intel Corporation, Hudson Jun 2008 - Aug 2008
Research Intern, Fault Aware Computing Technology Group
Performed redundancy analysis in modern Intel architectures, and worked on techniques for salvaging processor resources. The results were published in ISCA'09.

NEC Laboratories America, Princeton Jun 2007 - Aug 2007
Research Intern, System and Architecture Group
Proposed and implemented a novel hardware-assisted data race detection technique that leverages concepts from Transactional Memory. This work appears in SPAA'08 and IPDPS'09.

University of Michigan, Ann Arbor Sep 2006 - Dec 2006
Graduate Student Instructor, Department of EECS
Taught the undergraduate C++ data structures and algorithms course, EECS 280.

Technical University of Munich, Germany May 2004 - Jul 2004
Research Scholar, Institute of Electronic Design Automation
Designed a performance trade-off analysis and optimization tool for analog integrated circuits.

AWARDS AND HONORS

- Best paper award, *International Conference on Computer Design* 2009
- Graduate Fellowship from the EECS Department, University of Michigan, 2005-6
- *President of India Gold Medal*, Indian Institute of Technology Guwahati, 2005
- Institute Merit Scholarship, Indian Institute of Technology Guwahati, 2004
- Student Researcher Scholarship, Technical University of Munich, Germany, 2004

TECHNICAL SKILLS

Selected Project Experiences: Design and evaluation of microarchitectures and ISA, Compiler analysis and code transformations, Architectural power, area and energy modeling, Cache coherence protocol modifications, Modeling of wearout mechanisms and process variation, RTL level soft-error propagation analysis, ATPG design.

Compilers: Trimaran, LLVM.

Architectural Simulators: SIMICS, Liberty Simulation Environment, M5, ASIM, Simplescalar, Wisconsin GEMS, HotSpot, Wattch, CACTI.

CAD Tools: Synopsys Design Compiler, Physical Compier, Primetime, Cadence Encounter.

Programming Languages: C, C++, Java, Ruby, Verilog, Shell.

CONFERENCE PUBLICATIONS

[HPCA'11] A. Ansari, S. Feng, **S. Gupta**, S. Mahlke, *Archipelago: A Polymorphic Cache Design for Enabling Robust Near-Threshold Operation*, to appear in the Proceedings of the 17th International Symposium on High Performance Computer Architecture, February 2011.

[MICRO'10] **S. Gupta**, S. Feng, A. Ansari and S. Mahlke, *Erasing Core Boundaries for Robust and Configurable Performance*, in the Proceedings of the 43rd International Symposium on Microarchitecture, December 2010.

[DSN'10] **S. Gupta**, A. Ansari, S. Feng and S. Mahlke, *StageWeb: Interweaving Pipeline Stages into a Wearout and Variation Tolerant CMP Fabric*, in the Proceedings of the International Conference on Dependable Systems and Networks, June 2010.

[ISCA'10] A. Ansari, S. Feng, **S. Gupta**, S. Mahlke, *Necromancer: Enhancing System Throughput by Animating Dead Cores*, in the Proceedings of the International Symposium on Computer Architecture, June 2010.

[ASPLOS'10] S. Feng, **S. Gupta**, A. Ansari, and S. Mahlke, *Shoestring: Probabilistic Soft Error Reliability on the Cheap*, in the Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems, March 2010.

[HiPEAC'10] S. Feng, **S. Gupta**, A. Ansari, and S. Mahlke, *Maestro: Orchestrating Lifetime Reliability in Chip Multiprocessors*, in the Proceedings of the International Conference on High-Performance Embedded Architectures and Compilers, January 2010.

[MICRO'09] A. Ansari, **S. Gupta**, S. Feng and S. Mahlke, *ZerehCache: Armoring Cache Architectures in High Defect Density Technologies*, in the Proceedings of the 42nd International Symposium on Microarchitecture, December 2009.

[ICCD'09] **S. Gupta**, A. Ansari, S. Feng and S. Mahlke, *Adaptive Online Testing for Efficient Hard Fault Detection*, in the Proceedings of the 27th International Conference on Computer Design, October 2009. **(Best Paper Award)**

[ISLPED'09] A. Ansari, S. Feng, **S. Gupta**, and S. Mahlke, *Enabling Ultra Low Voltage System Operation by Tolerating On-Chip Cache Failures*, in the Proceedings of the International Symposium on Low Power Electronics and Design, August 2009.

[ISCA'09] M. D. Powell, A. Biswas, **S. Gupta** and S. S. Mukherjee, *Architectural Core Salvaging in a Multi-Core Processor for Hard-Error Tolerance*, in the Proceedings of the 36th International Symposium on Computer Architecture, June 2009.

[IPDPS'09] **S. Gupta**, F. Sultan, S. Cadambi, F. Ivancic and M. Roetteler, *Using Hardware Transactional Memory for Data Race Detection*, in the Proceedings of the 23rd International Parallel and Distributed Processing Symposium, May 2009.

[MICRO'08] **S. Gupta**, S. Feng, A. Ansari, J. Blome and S. Mahlke, *The StageNet Fabric for Constructing Resilient Multicore Systems*, in the Proceedings of the 41st Intl. Symposium on Microarchitecture, November 2008.

[CASES'08] **S. Gupta**, S. Feng, A. Ansari, J. Blome and S. Mahlke, *StageNetSlice: A Reconfigurable Microarchitecture Building Block for Resilient CMP Systems*, in the Proceedings of the Intl. Conference on Compilers, Architecture, and Synthesis for Embedded Systems, October 2008.
(Top Ranked Paper)

[MICRO'07] J. Blome, S. Feng, **S. Gupta**, S. Mahlke, *Self-calibrating Online Wearout Detection*, in the Proceedings of the 40th International Symposium on Microarchitecture, December 2007.
(Best Student Presentation Award)

[CASES'06] J. Blome, **S. Gupta**, S. Feng, S. Mahlke and D. Bradley, *Cost-Efficient Soft Error Protection for Embedded Microprocessors*, in the Proceedings of the Intl. Conference on Compilers, Architecture, and Synthesis for Embedded Systems, October 2006.

[ATS'05] **S. Gupta**, T. Vaish, and S. Chattopadhyay, *Flip-flop chaining architecture for power-efficient scan during test application*, in the Proceedings of the 14th Asian Test Symposium, December 2005.

JOURNAL PUBLICATIONS

S. Gupta, S. Feng, A. Ansari and S. Mahlke, *StageNet: A Reconfigurable Fabric for Constructing Dependable CMPs*, Special Issue on Dependable Systems, IEEE Transactions on Computers, 2011.

A. Ansari, **S. Gupta**, S. Feng and S. Mahlke, *Maximizing Spare Utilization by Virtually Reorganizing Faulty Cache Lines*, Special Issue on Dependable Systems, IEEE Transactions on Computers, 2011.

A. Ansari, S. Feng, **S. Gupta** and S. Mahlke, *Putting Faulty Cores to Work*, IEEE Micro, 2010.

S. Gupta, R. Tiwari and S. B. Nair, *Multi-objective Design Optimisation of Rolling Bearings using Genetic Algorithms*, in the Journal of Mechanism and Machine Theory, Vol 42/10 pp 1418-1443, Elsevier 2006.

SHORT PAPERS AND POSTERS

S. Gupta, S. Feng, A. Ansari, G. Dasika and S. Mahlke, *CoreGenesis: Erasing Core Boundaries for Robust and Configurable Performance*, To appear in Proceedings of the 19th International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2010.

S. Gupta, F. Sultan, S. Cadambi, F. Ivančić and M. Roetteler, *RaceTM: Detecting Data Races Using Transactional Memory*, in the Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), June 2008.

WORKSHOP ARTICLES

S. Feng, S. Gupta, and S. Mahlke, *Olay: Combat the Signs of Aging with Introspective Reliability Management*, in The Workshop on Quality-Aware Design, June 2008.

S. Gupta, S. Feng, J. Blome, and S. Mahlke, *StageNet: A Reconfigurable CMP Fabric for Resilient Systems*, in the 2^{nd} Reconfigurable and Adaptive Architecture Workshop, December 2007.

J. Blome, S. Feng, **S. Gupta**, S. Mahlke, *Online Timing Analysis for Wearout Detection*, in the 2nd Workshop on Architectural Reliability, December 2006.

S. Gupta, T. Vaish, and S. Chattopadhyay, *A Novel Approach to Reduce Test Power Consumption*, 8th IEEE VLSI Design and Test Workshop, August 2004.

TECHNICAL REPORTS

S. Gupta and S. Nandi, *Contention and drop-aware, traffic balancing, adaptive routing infrastructure for network-on-a-chip*, Bachelors' Thesis, Department of CSE, IIT Guwahati, April 2005.

S. Gupta, G. Stehr and H. Graeb, *On nonlinear determination of Pareto fronts*, Electronic Design Automation Institute, Technical University of Munich, Germany, July 2004.

GRANT PROPOSALS

- Toyota Research: *Software-only Detection and Recovery from Transient Faults*, 2010
- NSF: *An Adaptive Architecture Fabric for Constructing Resilient Multicore Systems*, 2008

SCHOLARLY PRESENTATIONS

- *Erasing Core Boundaries for Robust and Configurable Performance*, International Symposium on Microarchitecture, Atlanta, GA, December 2010

- *StageWeb: Interweaving Pipeline Stages into a Wearout and Variation Tolerant CMP Fabric*, International Conference on Dependable Systems and Networks, Chicago, IL, June 2010

- *Adaptive Online Testing for Efficient Hard Fault Detection*, Best Papers Session, International Conference on Computer Design, Lake Tahoe, CA, October 2009

- *The StageNet Fabric for Constructing Resilient Multicore Systems*
  - International Symposium on Microarchitecture, Lake Como, Italy, November 2008

- VSSAD Lunch Seminar, Intel Hudson, MA, June 2008

- *StageNetSlice: A Reconfigurable Microarchitecture Building Block for Resilient CMP Systems*, International Conference on Compilers, Architectures, and Synthesis for Embedded Systems, Atlanta, GA, October 2008

- *Exploiting Architectural Redundancy for Defect Tolerance*, Intern Day, Intel Hudson, MA, August 2008

- *RaceTM: Detecting Data Races Using Transactional Memory*, NEC Labs, Princeton, NJ, August 2007

- *Multicore Fault Tolerance*, NEC Labs, Princeton, NJ, June 2007

- *StageNet: A Reconfigurable CMP Fabric for Resilient Systems*, Reconfigurable and Adaptive Architecture Workshop (in conjunction with MICRO'07), Chicago, December 2007

- *CaDTARI: An Advanced NoC Infrastructure*, Undergraduate thesis talk, Indian Institute of Technology, Guwahati, India, April 2005

- *On Non-Linear Optimization of Analog Integrated Circuits*, Electronic Design and Automation Institute, Technical University of Munich, Germany, July 2004

PROFESSIONAL ACTIVITIES

- Reviewed papers for several architecture and compiler conferences: HPCA, ISCA, MICRO, ASPLOS, CASES, PACT, CODES/ISSS, CGO, DSN, HiPEAC, PLDI, DAC, DATE.
- Student member of IEEE and ACM.
- 2004-05 representative of Computer Science and Engineering Association, IIT Guwahati.

REFERENCES

Scott Mahlke
Associate Professor, EECS
University of Michigan, Ann Arbor
mahlke@umich.edu

Florin Sultan
Senior Research Scientist
Telcordia Technologies
sultan@dragon.rutgers.edu

Todd Austin
Professor, EECS
University of Michigan, Ann Arbor
austin@umich.edu

Valeria Bertacco
Associate Professor, EECS
University of Michigan, Ann Arbor
valeria@umich.edu

Zhengya Zhang
Assistant Professor, EECS
University of Michigan, Ann Arbor
zhengya@umich.edu

Michael D. Powell
Senior Design Engineer
Intel Corporation
michael.d.powell@intel.com